life.augmented

STISO620

Datasheet

Dual channel digital isolator

SO8N

Product status link

STISO620

Product label

SUSTAINABLE TECHNOLOGY

Features

- Dual channel digital isolator with 2 – 0 channel directionality
- High data rate up to 100 Mbps
- Wide T_{amb} range operation:- 40ºC to 125ºC
- High common-mode transient immunity
- From 3 V to 5.5 V supply levels
- Available in 8-pin SOIC narrow-body
- Low power consumption
- Pulse width distortions < 3ns
- Galvanic isolation
- Safety and regulatory approvals
  - UL1577 certified (V_{ISO} = 4kV pk), file number: E362869

Application

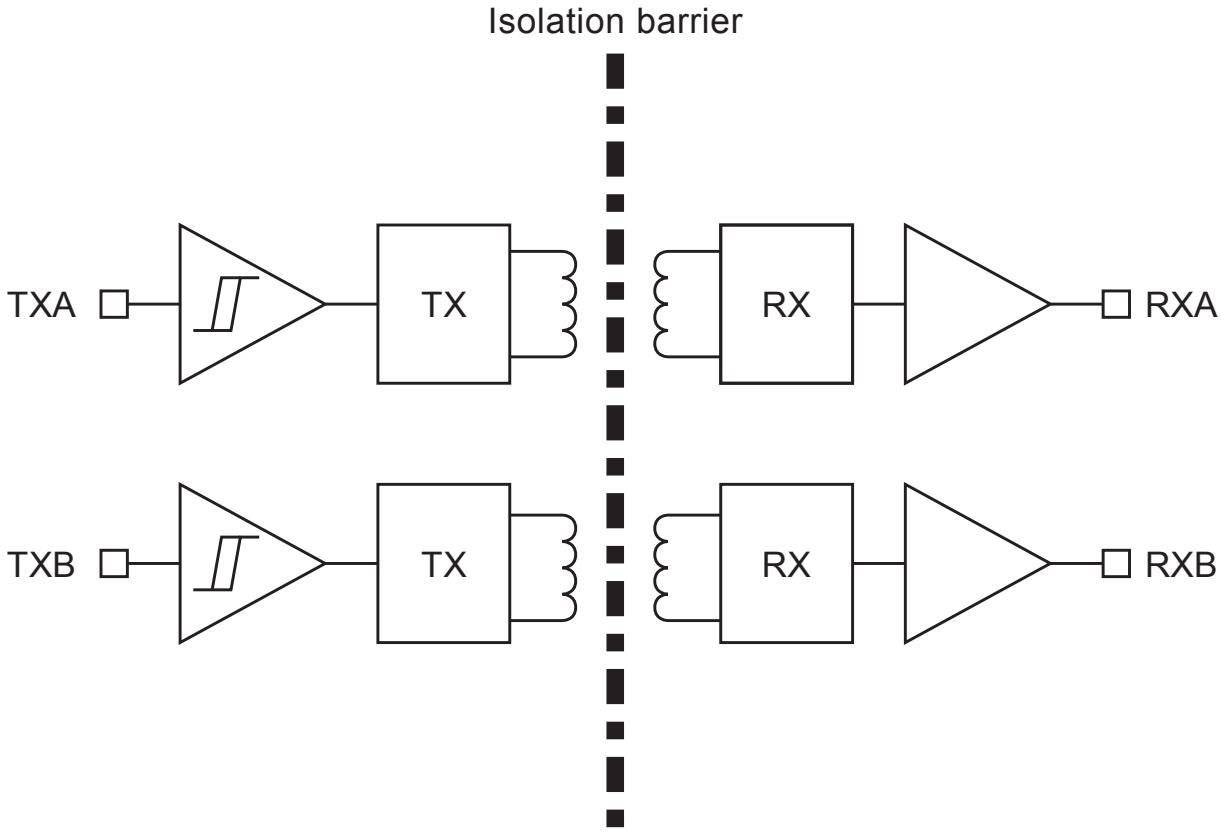
- Optocoupler replacement in industrial application
- Industrial field bus isolation
- Battery monitor and motor drive
- Size-critical multichannel isolation

Description

The STISO620 is a dual-channel digital isolator based on the ST thick oxide galvanic isolation technology. The device provides two independent channels in the same direction with Schmitt trigger input, providing robustness to noise and high speed input/output switching time.

1 Block diagram

Figure 1. **Block diagram**



2 Electrical data

2.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Test Condition	Value	Unit
V_{DDX}	Supply voltage (each side)		-0.3 to 5.5	V
V_{IN}	Logic input voltage		-0.3 to 5.5	V
I_O	Output current		5	mA
T_j	Junction temperature		-40 to 150	°C
T_{stg}	Storage temperature		-50 to 150	°C

2.2 Electrical sensitivity

Table 2. ESD protection ratings

Symbol	Parameter	Test Condition	Class	Value	Unit
HBM	Human Body Model	Conforming to ANSI/ESDA/JEDEC JS-001-2014		+/- 2	kV
CDM	Charge Device Model	All pins Conforming to ANSI/ESDA/JEDEC JS-002-2014		+/- 1000	V
MM	Machine Model	Conforming to EIA/JESD22-A115-C		+/- 200	V

2.3 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DDX}	Supply voltage (each side)		3		5.5	V
V_{IN}	Logic input voltage		0		5	V
T_{amb}	Ambient temperature		-40		125	°C

2.4 Electrical characteristics

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{DDXon}	V_{DDX} on threshold	V_{DDX} rising from 2 V to 3 V			2.75	V
$V_{DDXhyst}$	V_{DDX} off hysteresis	V_{DDX} falling from 5 V			0.2	V
I_{DD1}	Supply current (TX side)	DC		0.66	0.72	mA
		10 Mbps, 50 % duty cycle, C_L = 20 pF, VDD1 = 2.75 V		1.6	3	

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{DD1}	Supply current (TX side)	100 Mbps, 50 % duty cycle, C_L = 20 pF, VDD1 = 2.75 V		13	16	mA
		10 Mbps, 50 % duty cycle, C_L = 20 pF, VDD1 = 5 V		1.7	4	
		100 Mbps, 50 % duty cycle, C_L = 20 pF, VDD1 = 5 V		13	18	
I_{DD2}	Supply current (RX side)	DC		2.6	2.8	mA
		10 Mbps, 50 % duty cycle, C_L = 20 pF, VDD2 = 2.75 V		3.4	4.5	
		100 Mbps, 50 % duty cycle, C_L = 20 pF, VDD2 = 2.75 V		13	15	
		10 Mbps, 50 % duty cycle, C_L = 20 pF, VDD2 = 5 V		4.3	7	
		100 Mbps, 50 % duty cycle, C_L = 20 pF, VDD2 = 5 V		20	25	
V_{IHL}	Low level Schmitt trigger threshold	Logic input falling Full supply range	0.8			V
V_{ILH}	High level Schmitt trigger threshold	Logic input rising Full supply range			2	V
V_{OL}	Low level output voltage	I_{OH} = 4 mA			0.35	V
V_{OH}	High level output voltage	I_{OL} = 4 mA	V_{DDX} – 0.35			V
Z_O	Output impedance	T_{amb} = 25 °C V_{DD2} = 3.3 V	40	50	60	Ω
$f_{IN,MAX}$	Maximum data rate	V_{IH} = 5 V	100			Mbps
t_r	Output rise time	C_L = 20 pF T_{amb} = 25 °C See Figure 3		2		ns

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
t_f	Output fall time	C_L = 20 pF T_{amb} = 25 °C See Figure 3		2		ns
t_{DHL}	Propagation delay H to L	Tamb = 25°C See Figure 3		25		ns
		Full temperature range			42	
t_{DLH}	Propagation delay L to H	Tamb = 25°C See Figure 3		25		ns
		Full temperature range			42	
t_{POWUP}	Power up time				30	µs
$t_{REFRESH}$	Refresh time			1	2	µs
t_{WD}	Watchdog timeout		2		8	µs
PWD	Pulse width distortion $\lvert t_{DHL} - t_{DLH} \rvert$	Tamb = 25°C		1.7	2.6	ns
		Full temperature range			3	
CMTI	Common mode transient immunity	(1)	50	65		kV/µs

1. *Not tested in production. Limit is guaranteed by characterization on a limited number of samples and simulations.*

Note: ***Testing conditions: Typical values are defined at Tamb = 25°C and VDD1 = VDD2 = 3 V, minimum and maximum limits applies to the full temperature range (Tested in production at T_{amb} = 25°C and the limits in the full temperature range are guaranteed by characterization on a limited quantity of samples), unless otherwise specified.***

3 Isolation characteristics

Table 5. Isolation specifications

Parameter	Symbol	Conditions	Value	Unit
Clearance (Minimum external air gap)	CLR	Measured from input terminals to output terminals, shortest distance through air	4	mm
Creepage (Minimum external tracking)	CPG	Measured from input terminals to output terminals, shortest distance path along body	4	mm
Comparative Tracking Index (Tracking resistance)	CTI	DIN IEC 112/VDE 0303 Part 1	≥ 400	V
Isolation Group		Material Group (DIN VDE 0110, 1/89, Table 1)	II	

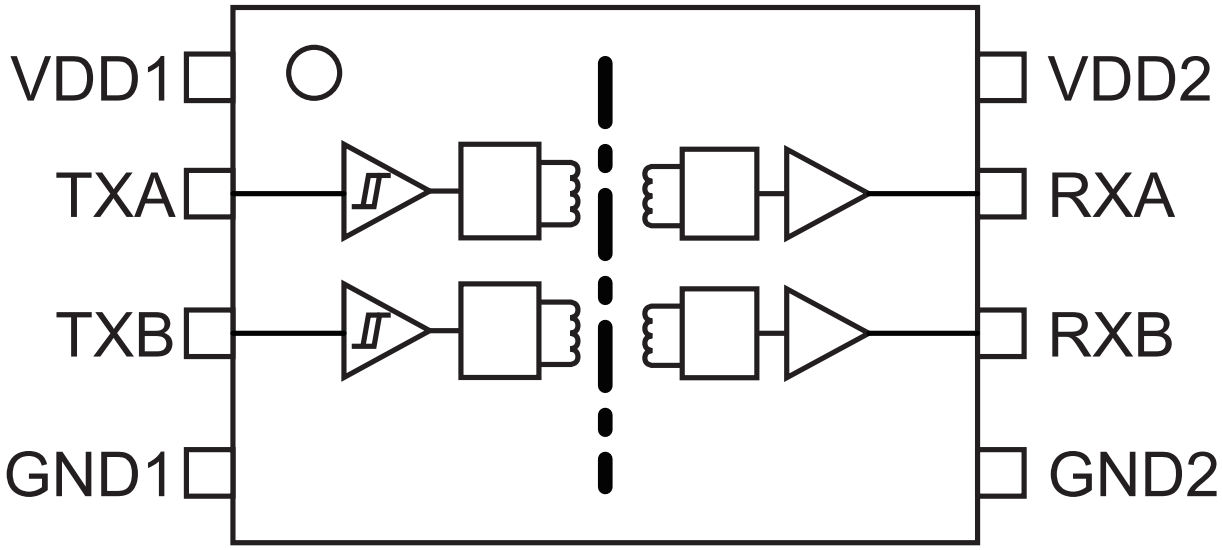
Table 6. Isolation characteristics

Parameter	Symbol	Test Conditions	Characteristic	Unit
Maximum working isolation voltage	V_{IORM}		1200	V_{PEAK}
Input to output test voltage	V_{PR}	Method a, Type test (1) $V_{PR} = V_{IORM} \times 1.6$, t_m= 10 s Partial discharge < 5 pC	1920	V_{PEAK}
		Method b, 100 % Production test (1) $V_{PR} = V_{IORM} \times 1.875$, t_m = 1 s Partial discharge < 5 pC	2250	V_{PEAK}
Isolation withstand voltage	V_{ISO}	1min (Type test) (2)	2830/4000	V_{rms} /V_{PEAK}
Isolation test voltage	$V_{ISOtest}$	1sec (100% production) (2)	3395/4800	V_{rms} /V_{PEAK}
Transient overvoltage (Highest allowable overvoltage)	V_{IOTM}	t_{ini}= 60 s Type test (1)	4000	V_{PEAK}
Maximum surge isolation voltage	V_{IOSM}	Type test (1)	4000	V_{PEAK}
Isolation resistance	R_{IO}	V_{IO} = 500 V at T_S	>10^9	Ω

1. *Test performed in accordance with IEC 60747-5-2*
2. *Test performed in accordance with UL 1577*

4 Pin connection

Figure 2. **Pin connection (top view)**



5 Pin list

Table 7. **Pin description**

N.	Name	Type	Function
1	VDD1	Supply	Supply voltage side 1
2	TXA	Logic input	Transmit data channel A
3	TXB	Logic input	Transmit data channel B
4	GND1	Ground	Ground side 1
5	GND2	Ground	Ground side 2
6	RXA	Logic output	Receive data channel A
7	RXB	Logic output	Receive data channel B
8	VDD2	Supply	Supply voltage side 2

6 Device description

The STISO620 is a dual high-speed isolated communication channel. It integrates two channels in the same direction and provides low levels of pulse width distortion in the full operation range.

6.1 Device operation

The device operation is described in the following table:

Table 8. Device operation table

VDD1	VDD2	Tx	Rx
Above UVLO	Above UVLO	H	H
		L	L
Below UVLO	Above UVLO	X	L(1)
Above UVLO	Below UVLO	X	Tri-state
Below UVLO	Below UVLO	X	Tri-state

1. *Safe state imposed by default.*

When both sides of the device are powered (above UVLO threshold), the device operates as an isolated buffer between the Tx input, and the respective Rx output (see Figure 3).

Figure 3. Timing diagram

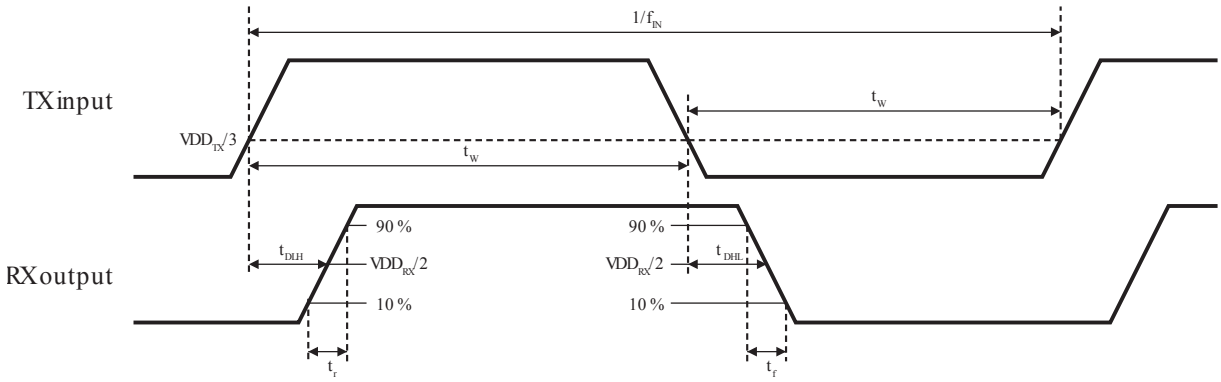
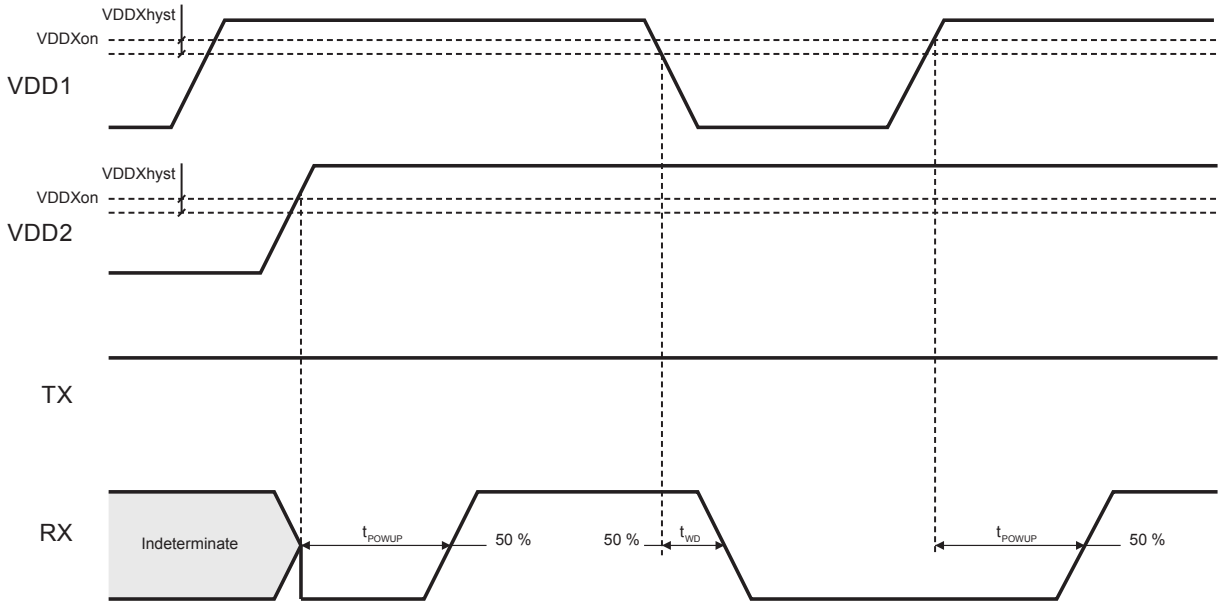


Figure 4. **Timing diagram – power-up and power-down**



7 Characterization graphs

Following data are based on characterization tests on a limited number of samples.

Figure 5. tr/tf thermal drift normalized at 25°C

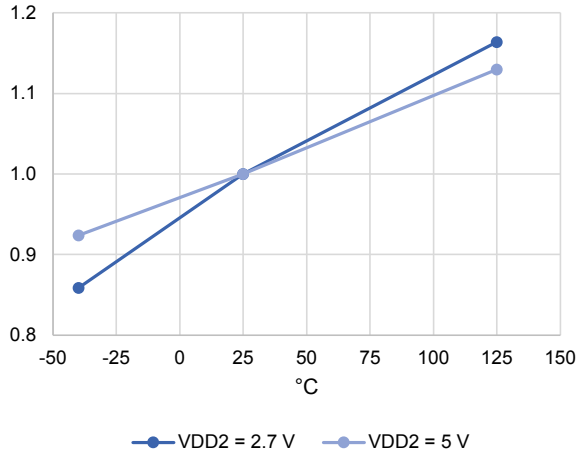
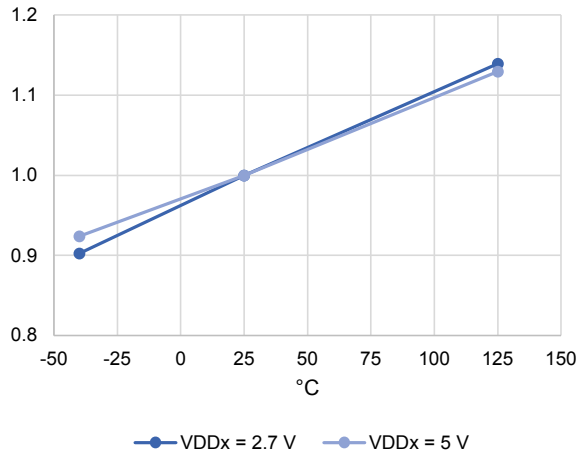


Figure 6. Propagation delay thermal drift normalized at 25°C



8 Package mechanical data

Table 9. **SO8 narrow package dimensions**

Symbol	Min.	Nom.	Max.
A	1.35		1.75
A1	0.10		0.25
b	0.35		0.49
c	0.19		0.25
D	4.80		5.00
e		1.27BSC	
E1	3.80		4.00
E	5.80		6.20
L	0.40		1.25
h	0.25		0.50
θ	0°		7°
Θ1	2°		12*
aaa		0.25	
bbb		0.25	
ccc		0.10	

Figure 7. **SO8 package drawings**

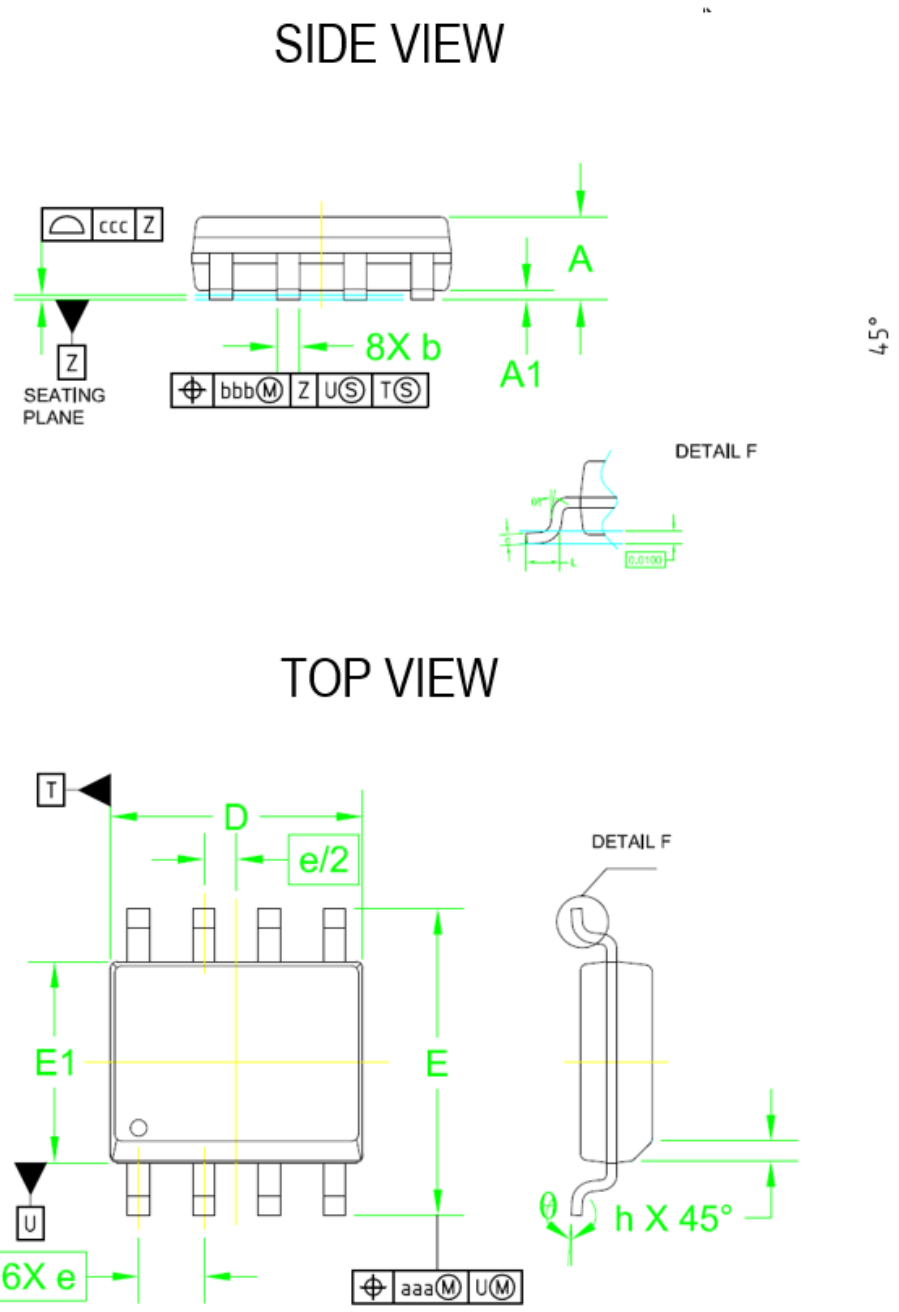
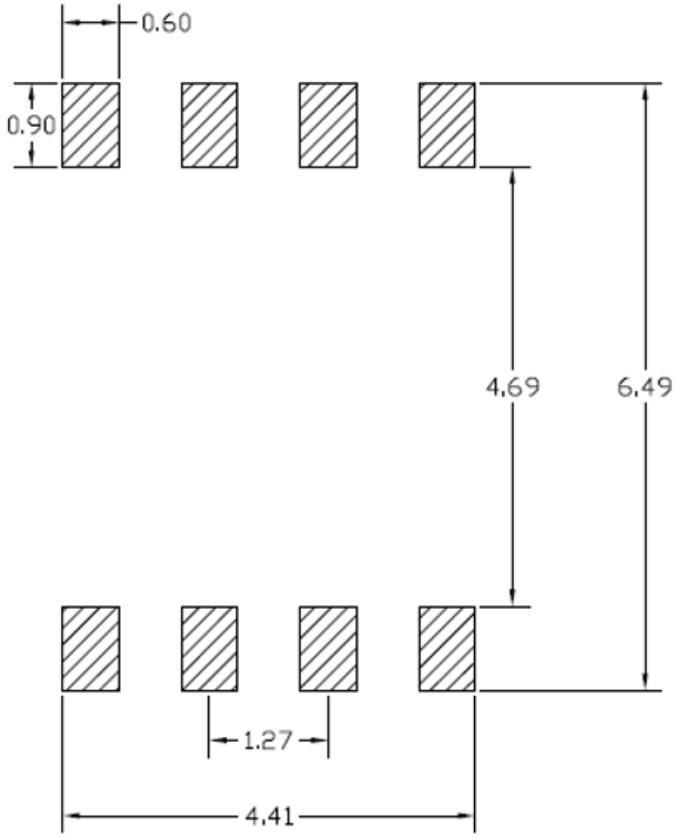


Figure 8. **SO8 package recommended footprint**



9 Order Information

Table 10. **Order Information**

Order Code	Package	Packing
STISO620	S08 narrow body	Tray
STISO620TR	S08 narrow body	Tape and Reel

Revision history

Table 11. **Document revision history**

Date	Version	Changes
07-Nov-2022	1	Initial release.

Contents

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