

EPC2304 – Enhancement Mode Power Transistor

V_{DS} , 200 V

$R_{DS(on)}$, 3.1 mΩ typ

PRELIMINARY



RoHS

Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source
- Questions: [Ask a GaN Expert](#)

Questions:

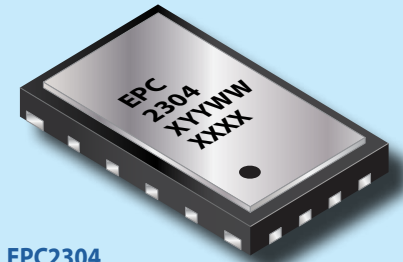


| Maximum Ratings | | | |
|-----------------|---|------------|------|
| PARAMETER | | VALUE | UNIT |
| V_{DS} | Drain-to-Source Voltage (Continuous) | 200 | V |
| | Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C) | 240 | |
| I_D | Continuous ($T_A = 25^\circ\text{C}$) | 102 | A |
| | Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$) | 260 | |
| V_{GS} | Gate-to-Source Voltage | 6 | V |
| | Gate-to-Source Voltage | -4 | |
| T_J | Operating Temperature | -40 to 150 | °C |
| T_{STG} | Storage Temperature | -40 to 150 | |

| Thermal Characteristics | | | |
|-------------------------|--|-----|------|
| PARAMETER | | TYP | UNIT |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | 0.2 | °C/W |
| $R_{\theta JB}$ | Thermal Resistance, Junction-to-Board | 1.5 | |
| $R_{\theta JA_JEDEC}$ | Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB) | 45 | |
| $R_{\theta JA_EVB}$ | Thermal Resistance, Junction-to-Ambient (using EPC90140 EVB) | 21 | |

| Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated) | | | | | | |
|--|---|---|-----|-------|-----|------|
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
| BV_{DSS} | Drain-to-Source Voltage | $V_{GS} = 0\text{ V}$, $I_D = [\text{TBD}]$ | 200 | | | V |
| I_{DSS} | Drain-Source Leakage | $V_{GS} = 0\text{ V}$, $V_{DS} = 160\text{ V}$ | | 0.003 | | mA |
| I_{GSS} | Gate-to-Source Forward Leakage | $V_{GS} = 5\text{ V}$ | | 0.011 | | |
| | Gate-to-Source Forward Leakage [#] | $V_{GS} = 5\text{ V}$, $T_J = 125^\circ\text{C}$ | | 0.8 | | |
| | Gate-to-Source Reverse Leakage | $V_{GS} = -4\text{ V}$ | | 0.005 | | |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}$, $I_D = 8\text{ mA}$ | 0.8 | 1.1 | 2.5 | V |
| $R_{DS(on)}$ | Drain-Source On Resistance | $V_{GS} = 5\text{ V}$, $I_D = 32\text{ A}$ | | 3.1 | | mΩ |
| V_{SD} | Source-Drain Forward Voltage [#] | $I_S = 0.5\text{ A}$, $V_{GS} = 0\text{ V}$ | | 1.6 | | V |

[#] Defined by design. Not subject to production test.



EPC2304

Package size: 3 x 5 mm

Applications

- Synchronous Rectification
- AC/DC Chargers, SMPS, Adaptors
- High Frequency DC-DC Conversion
- Class D audio
- Wireless Power
- High Power Lidar & dToF

Benefits

- Higher Efficiency – Lower conduction and switching losses, zero reverse recovery losses
- Ultra Small Footprint – Higher power density

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2304>

Dynamic Characteristics# (T_j = 25°C unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------|---|---|-----|------|-----|------|
| C _{ISS} | Input Capacitance | V _{DS} = 100 V, V _{GS} = 0 V | | 3195 | | pF |
| C _{RSS} | Reverse Transfer Capacitance | | | 2.7 | | |
| C _{OSS} | Output Capacitance | | | 649 | | |
| C _{OSS(ER)} | Effective Output Capacitance, Energy Related (Note 1) | V _{DS} = 0 to 100 V, V _{GS} = 0 V | | 852 | | pF |
| C _{OSS(TR)} | Effective Output Capacitance, Time Related (Note 2) | | | 1156 | | |
| R _G | Gate Resistance | | | 0.4 | | Ω |
| Q _G | Total Gate Charge | V _{DS} = 100 V, V _{GS} = 5 V, I _D = 32 A | | 24 | | nC |
| Q _{GS} | Gate-to-Source Charge | V _{DS} = 100 V, I _D = 32 A | | 7.6 | | |
| Q _{GD} | Gate-to-Drain Charge | | | 2.5 | | |
| Q _{G(TH)} | Gate Charge at Threshold | | | 5 | | |
| Q _{OSS} | Output Charge | V _{DS} = 100 V, V _{GS} = 0 V | | 116 | | |
| Q _{RR} | Source-Drain Recovery Charge | | | 0 | | |

Defined by design. Not subject to production test.

All measurements were done with substrate shorted to source.

Note 1: C_{OSS(ER)} is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
 Note 2: C_{OSS(TR)} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

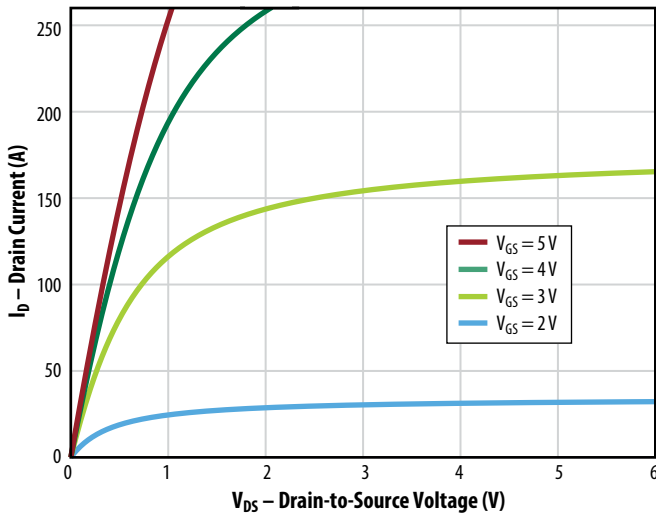


Figure 2: Typical Transfer Characteristics

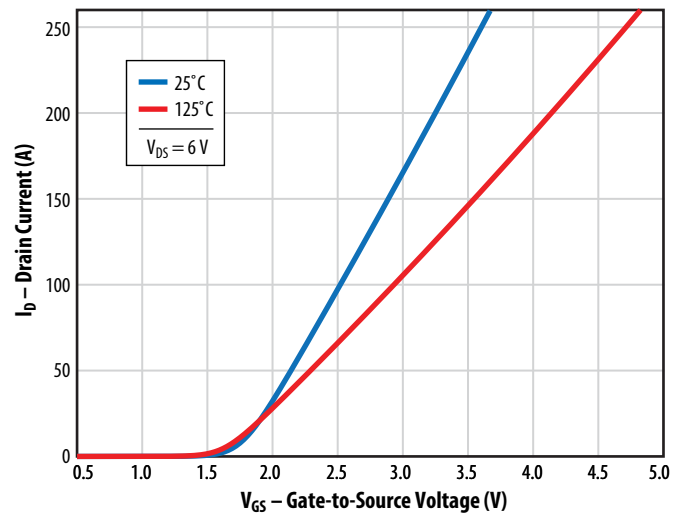


Figure 3: Typical R_{DS(on)} vs. V_{GS} for Various Drain Currents

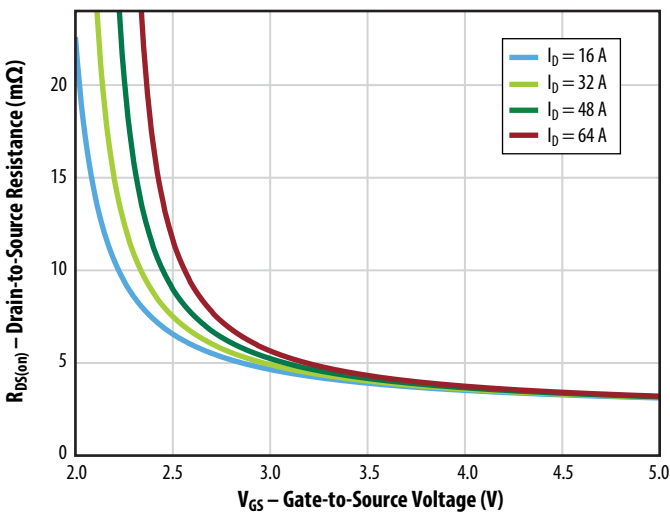


Figure 4: Typical R_{DS(on)} vs. V_{GS} for Various Temperatures

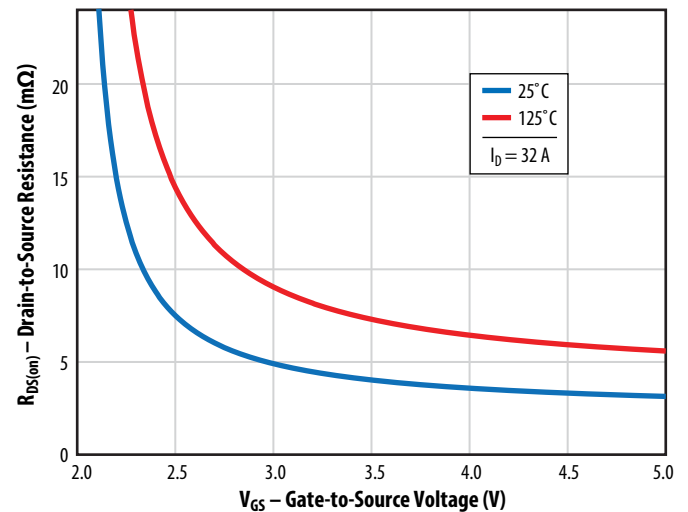


Figure 5a: Typical Capacitance (Linear Scale)

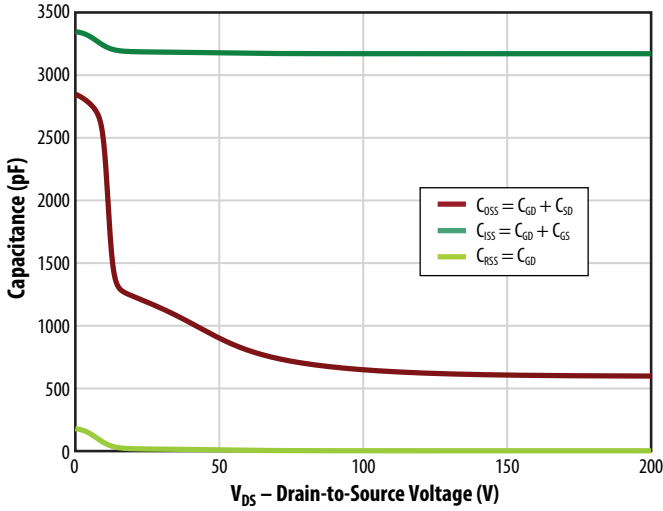


Figure 5b: Typical Capacitance (Log Scale)

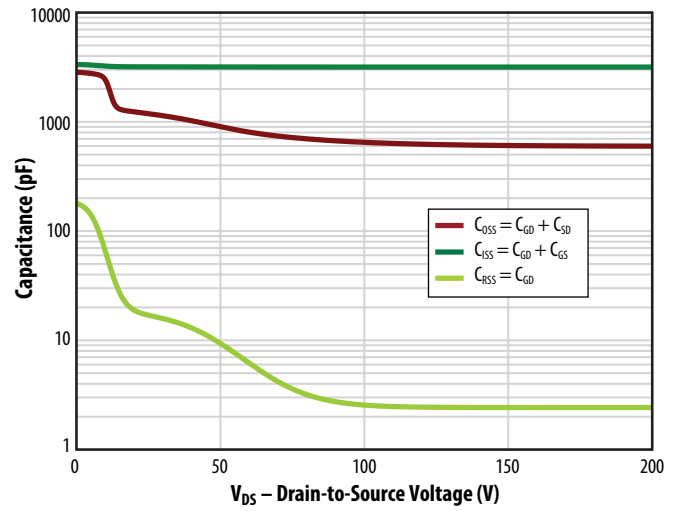


Figure 6: Typical Output Charge and C_OSS Stored Energy

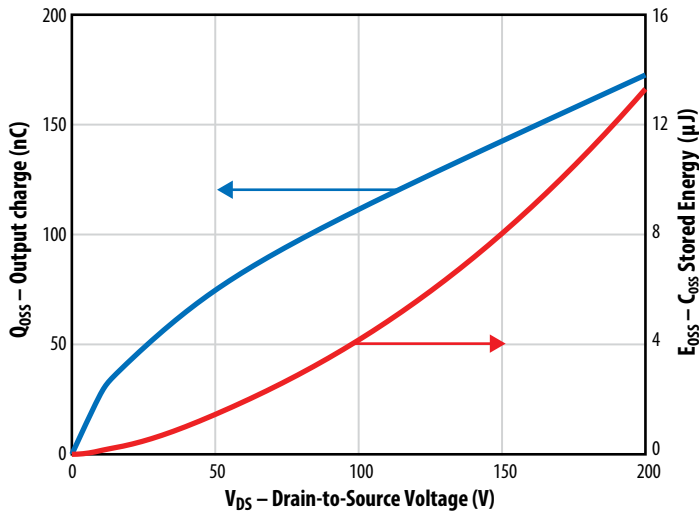


Figure 7: Typical Gate Charge

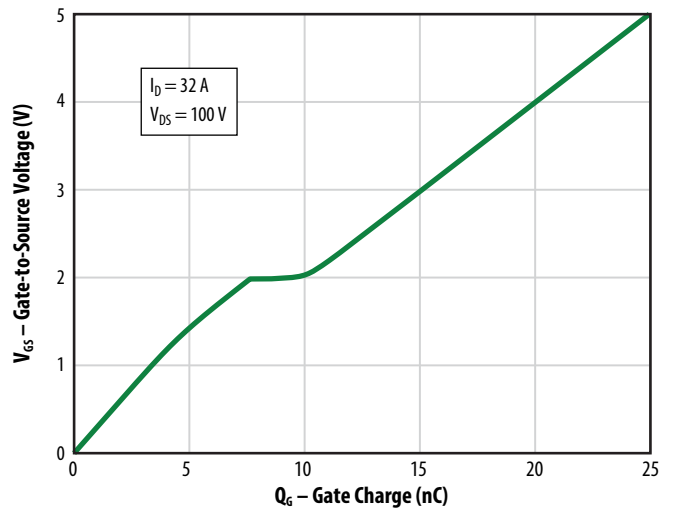
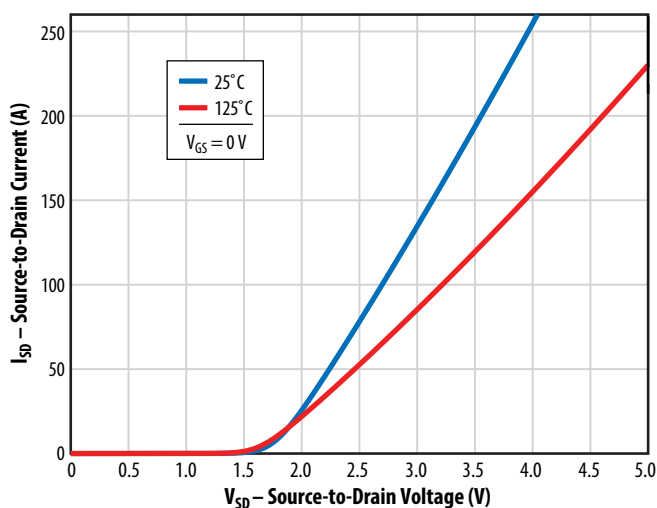


Figure 8: Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0V for OFF.

Figure 9: Typical Normalized On-State Resistance vs. Temp.

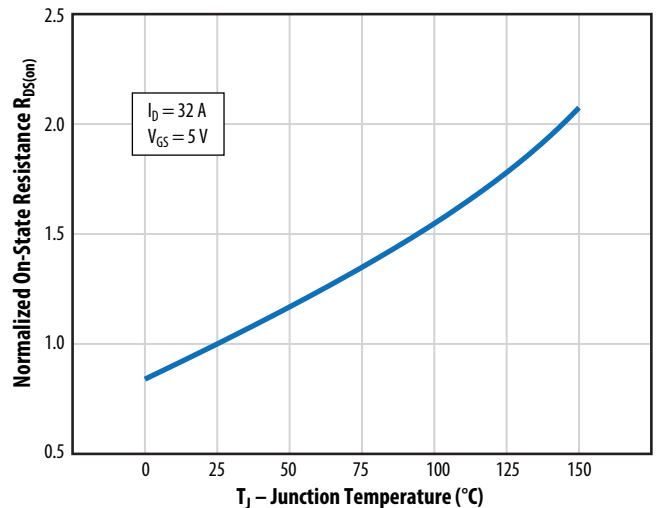


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

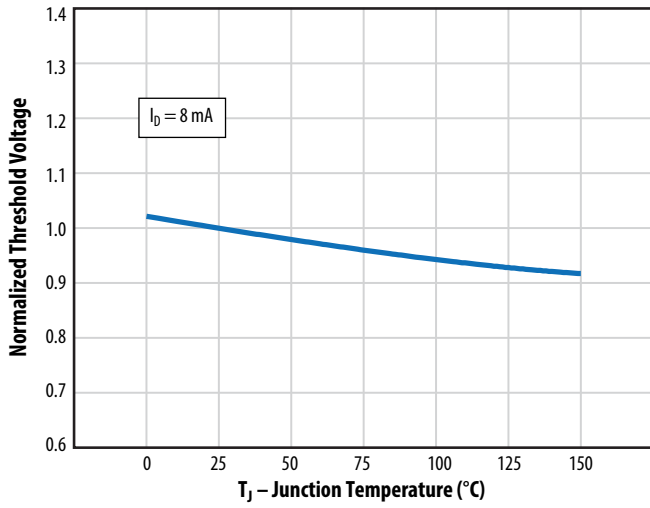


Figure 11: Safe Operating Area

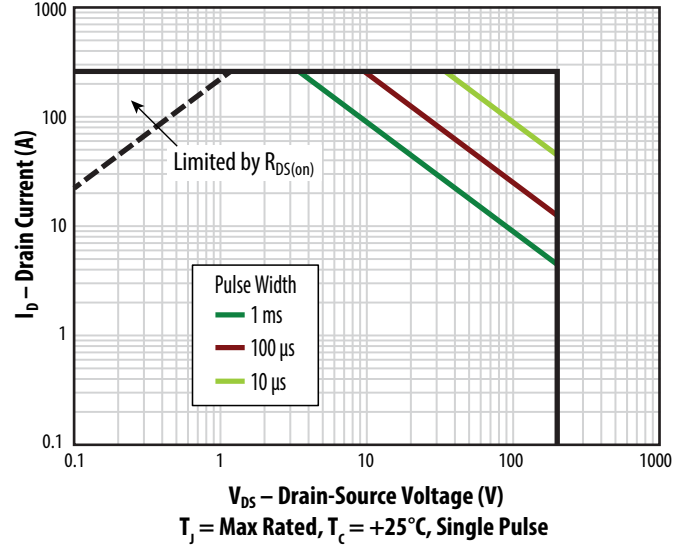
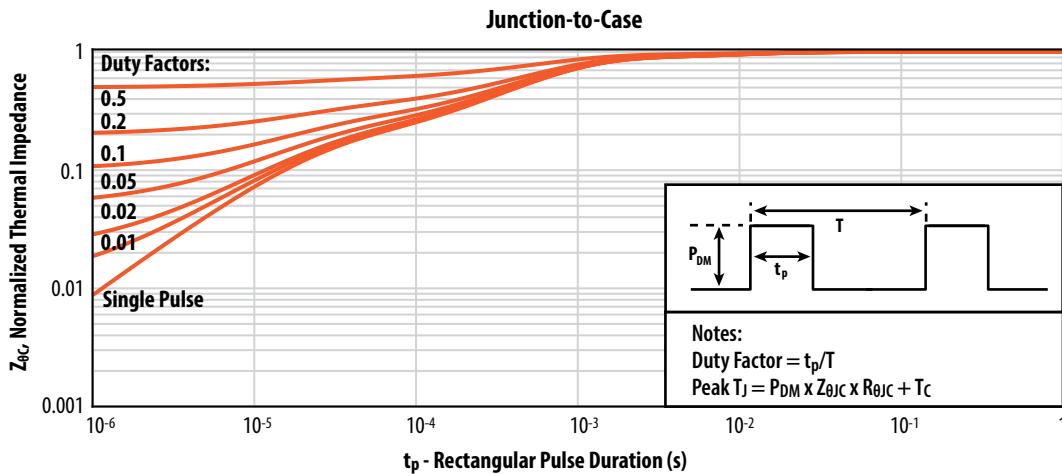
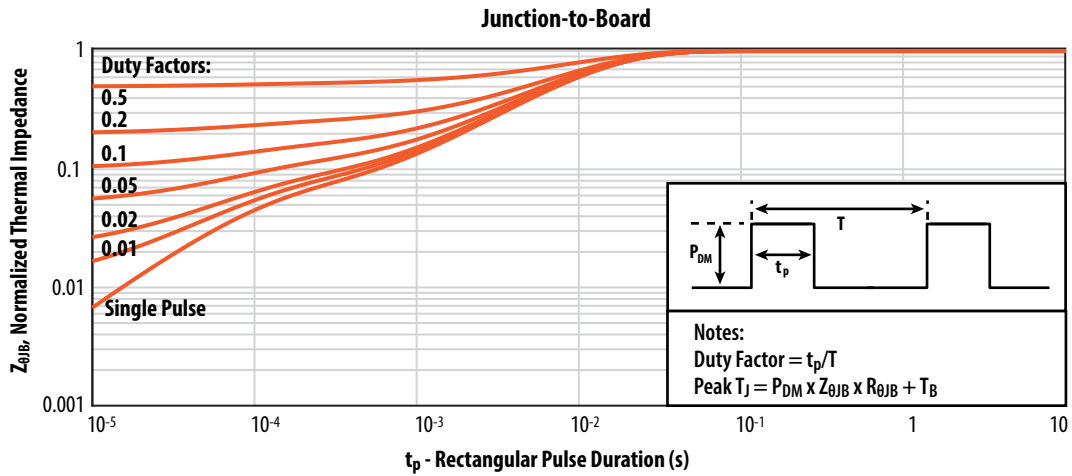
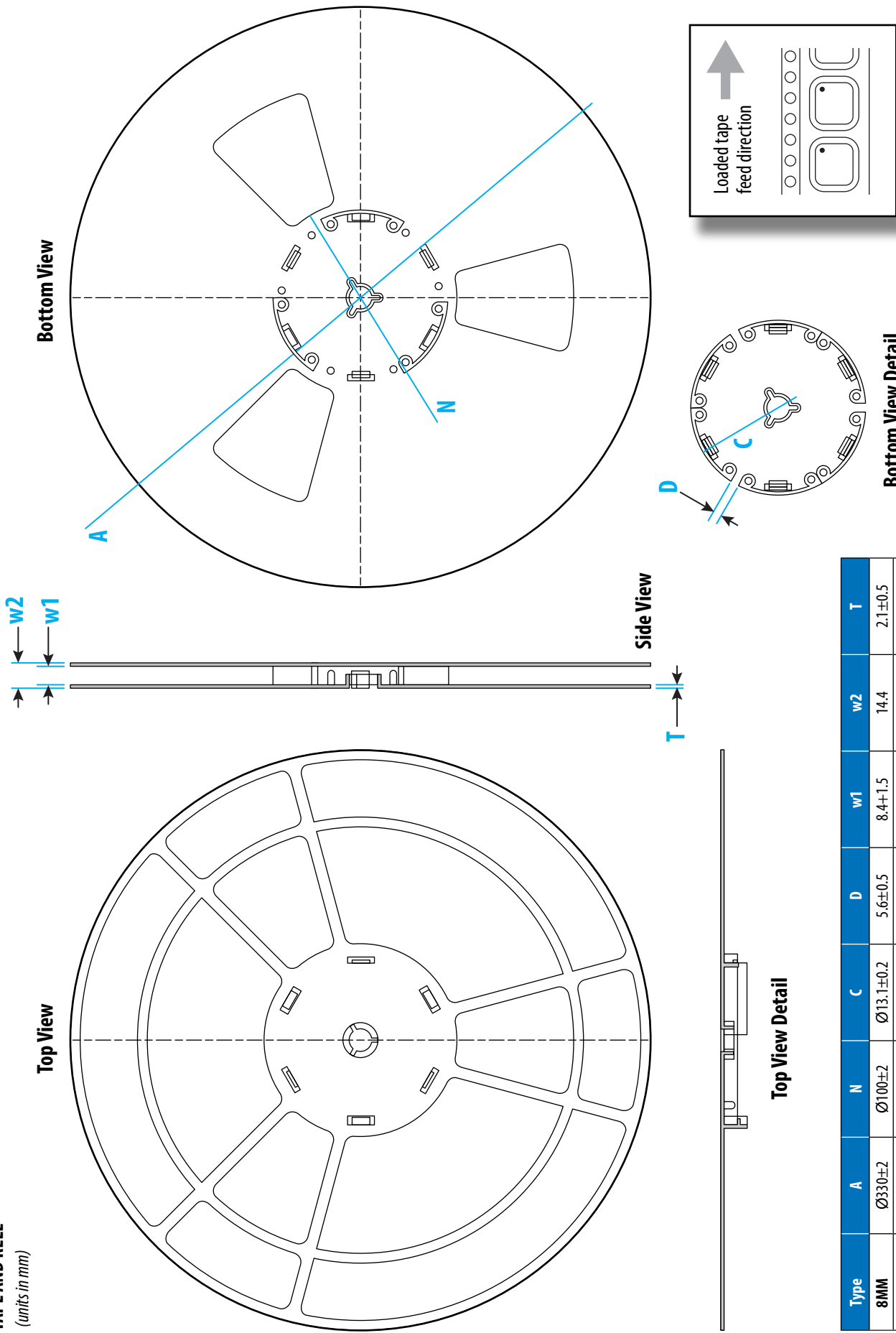


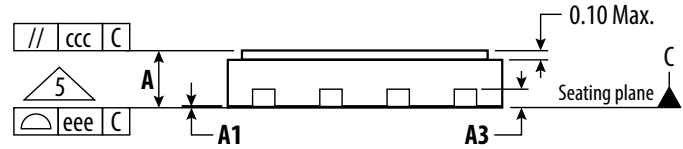
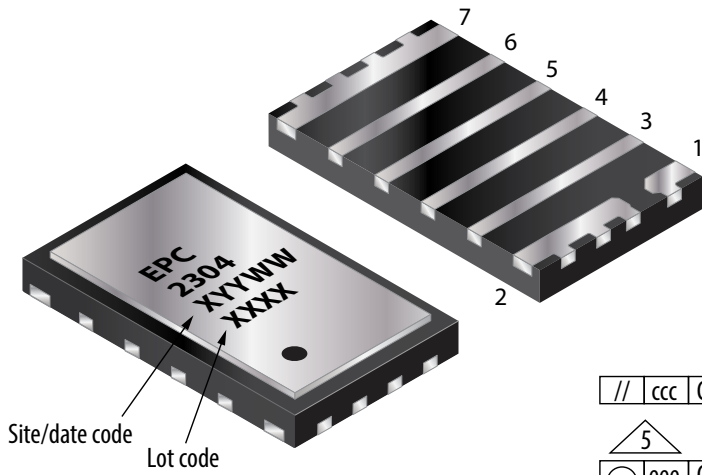
Figure 12: Transient Thermal Response Curves



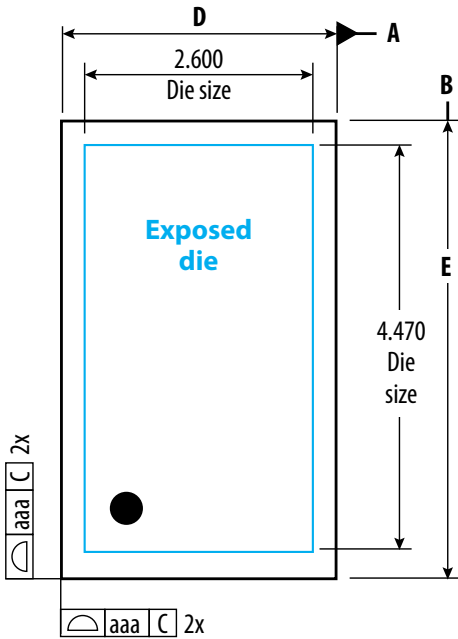
TAPE AND REEL
(units in mm)



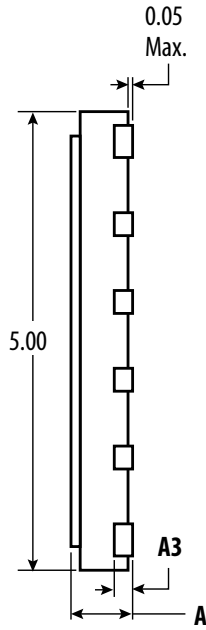
| Type | A | N | C | D | w1 | w2 | T |
|------|-------------------------|-------------------------|----------------------------|---------------|----------------|------|---------------|
| 8MM | $\varnothing 330 \pm 2$ | $\varnothing 100 \pm 2$ | $\varnothing 13.1 \pm 0.2$ | 5.6 ± 0.5 | 8.4 ± 1.5 | 14.4 | 2.1 ± 0.5 |
| 12MM | $\varnothing 330 \pm 2$ | $\varnothing 100 \pm 2$ | $\varnothing 13.1 \pm 0.2$ | 5.6 ± 0.5 | 12.4 ± 1.5 | 18.4 | 2.1 ± 0.5 |
| 16MM | $\varnothing 330 \pm 2$ | $\varnothing 100 \pm 2$ | $\varnothing 13.1 \pm 0.2$ | 5.6 ± 0.5 | 16.4 ± 1.5 | 22.4 | 2.1 ± 0.5 |
| 24MM | $\varnothing 330 \pm 2$ | $\varnothing 100 \pm 2$ | $\varnothing 13.1 \pm 0.2$ | 5.6 ± 0.5 | 24.4 ± 1.5 | 30.4 | 2.1 ± 0.5 |



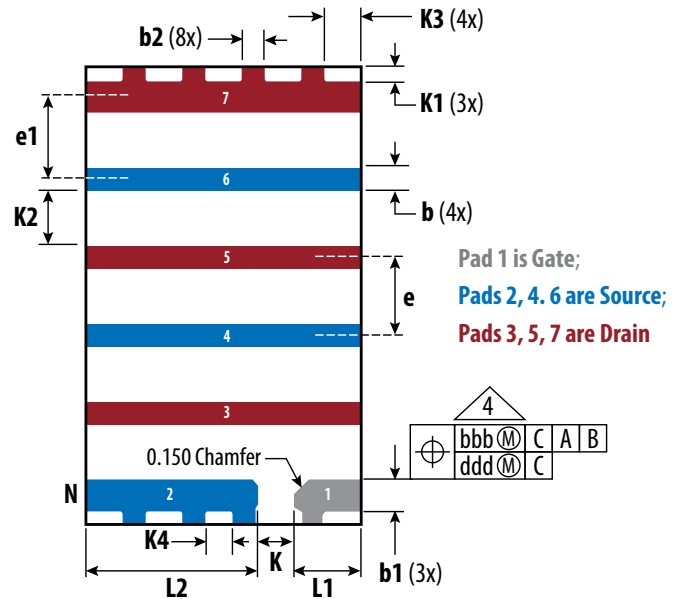
Side View 2



Top View



Side View 1



Bottom View

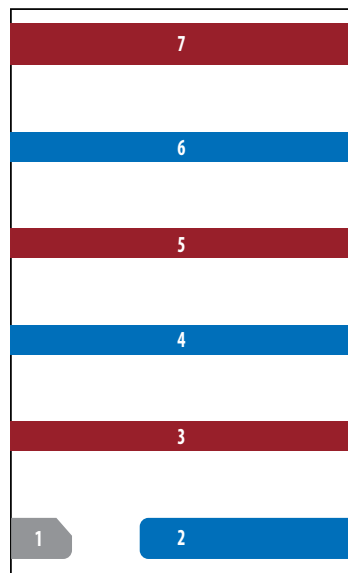
| SYMBOL | Dimension (mm) | | | Note |
|--------|----------------|----------|-------|------|
| | MIN | Nominal | MAX | |
| A | 0.60 | 0.65 | 0.70 | |
| A1 | 0.00 | 0.02 | 0.05 | |
| A3 | | 0.20 Ref | | |
| b | 0.20 | 0.25 | 0.30 | 4 |
| b1 | 0.30 | 0.35 | 0.40 | 4 |
| b2 | 0.20 | 0.25 | 0.30 | 4 |
| D | | 3.00 BSC | | |
| E | | 5.00 BSC | | |
| e | | 0.85 BSC | | |
| e1 | | 0.90 BSC | | |
| L1 | 0.625 | 0.725 | 0.825 | |
| L2 | 1.775 | 1.875 | 1.975 | |

| SYMBOL | Dimension (mm) | | | Note |
|--------|----------------|---------|------|------|
| | MIN | Nominal | MAX | |
| K | 0.35 | 0.40 | 0.45 | |
| K1 | 0.10 | 0.15 | 0.20 | |
| K2 | 0.55 | 0.60 | 0.65 | |
| K3 | 0.35 | 0.40 | 0.45 | |
| K4 | 0.25 | 0.30 | 0.35 | |
| aaa | | 0.05 | | |
| bbb | | 0.10 | | |
| ccc | | 0.10 | | |
| ddd | | 0.05 | | |
| eee | | 0.08 | | |
| N | | 15 | | 3 |
| NE | | 6 | | |

Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. N is the total number of terminals
4. Dimension b applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
5. Coplanarity applies to the terminals and all the other bottom surface metallization.

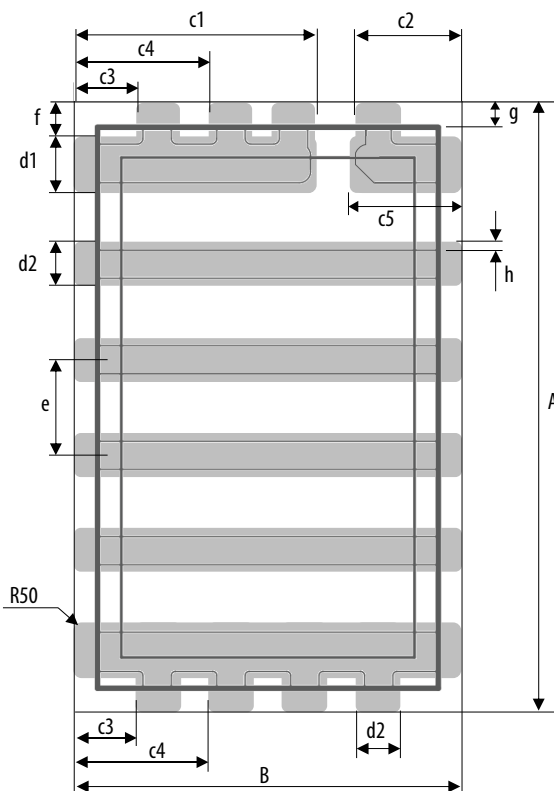
TRANSPARENT VIEW



Transparent Top View

| PIN | DESCRIPTION |
|-----|-------------|
| 1 | Gate |
| 2 | Source |
| 3 | Drain |
| 4 | Source |
| 5 | Drain |
| 6 | Source |
| 7 | Drain |

RECOMMENDED LAND PATTERN
(units in mm)



Land pattern is solder mask defined.
It is recommended to have on-Cu trace PCB vias.

| DIM | Nominal |
|-----|---------|
| A | 5.4 |
| B | 3.4 |
| c1 | 2.1 |
| c2 | 0.90 |
| c3 | 0.55 |
| c4 | 1.20 |
| c5 | 0.975 |
| d1 | 0.45 |
| d2 | 0.35 |
| e | 0.85 |
| f | 0.30 |
| g | 0.2 |
| h | 0.05 |

Additional Resources Available:

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – <https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip>
(for preliminary device Altium footprints, contact EPC)

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