Preliminary

LTC4296-1

5-Port SPoE PSE Controller

FEATURES

- **IEEE 802.3cg Compliant SPoE PSE**
- **Five Independent PSE Ports**
- **Wide Input Voltage Range: 6V to 60V**
- **Adjustable Source and Return Electronic Circuit Breakers**
- **50µA (typ) Supply Current in Deep Sleep/Disabled**
- Charge Pump Enhances External High-Side N-Channel MOSFET
- Supports PD Classification with a Microcontroller
- SPI Bus Interface with PEC
- Voltage, Current, and Temperature Telemetry
- Per Port Power Good Comparators
- PD Sleep, Wakeup, and Wakeup Forwarding Support
- Available in 48-lead 7mm × 7mm QFN Package

APPLICATIONS

- Operational Technology (OT) Systems
- Building and Factory Automation Systems
- Field instruments and switches
- Security Systems
- Traffic Control Systems

DESCRIPTION

The LTC®4296-1 is an IEEE 802.3cg compliant five port Single-pair Power over Ethernet (SPoE) Power Sourcing Equipment (PSE) controller. SPoE simplifies system design and installation with standardized power and Ethernet data over a single-pair cable. The LTC4296-1 is designed for interoperability with 802.3cg Powered Devices (PDs) in 24V or 54V systems. It delivers power using external, low $R_{DS(ON)}$, N-channel MOSFETs which minimize voltage drop and ensure application ruggedness.

High-side circuit breakers with foldback Analog Current Limit (ACL) provide controlled inrush and short circuit protection. An optional low-side circuit breaker protects the negative output against back-feed faults, and ground faults in non-isolated applications. PD classification and Maintain Full Voltage Signature (MFVS) ensure full operating voltage is only applied to the cable when a PD is present. SWn pins disconnect port power snubbers during detection and classification. PD initiated sleep and wakeup are supported. The WAKEUP pin supports wakeup forwarding. Telemetry, status, and software control features are accessed via a SPI bus interface with Packet Error Code (PEC) protection.

The LTC4296-1 provides a versatile SPoE PSE solution for 10BASE-T1L controllers and switches and can easily be integrated with the ADI 10BASE-T1L transceiver portfolio such as the ADIN1100 (PHY), ADIN1110 (MAC-PHY) and ADIN2111 (2-Port switch).

TYPICAL APPLICATION

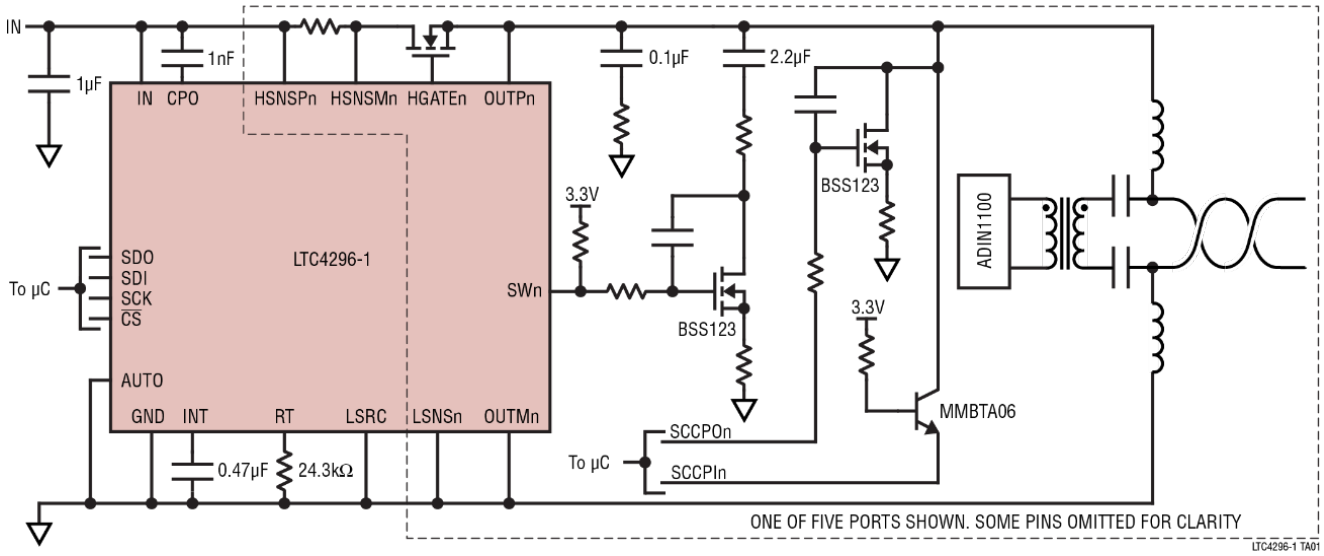

Figure 1. IEEE 802.3cg Compliant PSE

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ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3, 4, 5)

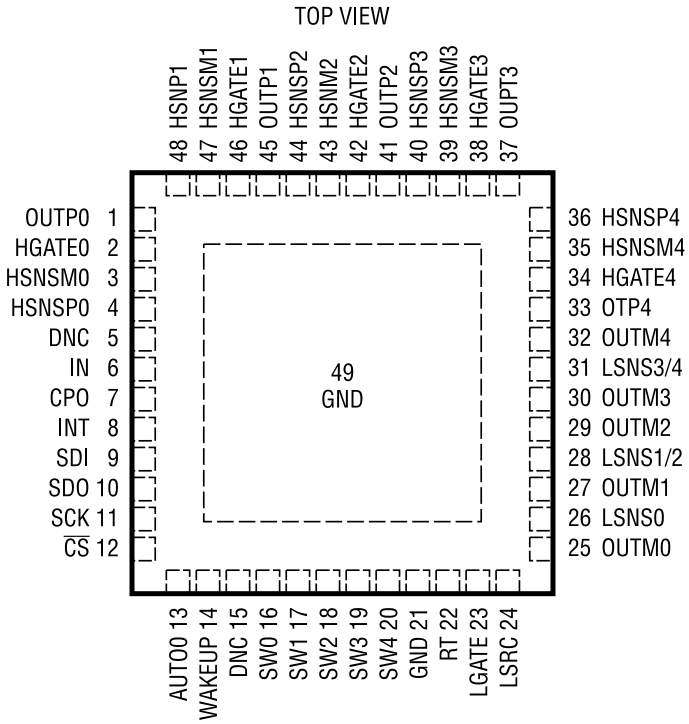
Table 1.

PARAMETER	RATING
Supply Voltage	
IN	–0.3V to 80V
INT	–0.3V to 6V
Input Voltages	
SDI, SCK, $\overline{CS}$, AUTO, RT	–0.3V to 6V
HSNSPn, HSNSMn	–0.3V to 80V
HSNSPn to HSNSMn	–5V to 10V
OUTMn	–5.5V to 80V
LSNSn	–5.5V to 80V
OUTPn	–5.5V to 80V
Output Voltages	
SDO, WAKEUP, SWn	–0.3V to 6V
LGATE to LSRC	–0.3V to 15V
LSRC	–5.5V to 4V
CPO to IN	–0.3V to 15V
HGATEn to OUTPn	–0.3V to 15V
Output Currents	
SDO, SWn	±5mA
RT	–10mA to 1mA
Operating Junction Temperature Range	–40 to 125°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



UK PACKAGE
48-LEAD (7mm × 7mm) PLASTIC QFN
θ_{JC} = 2.5°C/W, θ_{JA} = 18°C/W
EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB

ELECTRICAL CHARACTERISTICS

The * denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 6V and 60V unless otherwise noted.

Table 2.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN							
V_{IN}	Input Supply Operating Range		*	6		60	V
I_{IN}	Input Supply Current	All Ports in POWER_ON State	*		6.5	10	mA
		All Ports in SLEEP State, Serial Bus Idle	*		52	140	µA
		All Ports in DISABLED State, Serial Bus Idle	*		51	135	µA
		All Ports in DETECTION State	*		80	90	mA
INT							
V_{INT}	INT Voltage	I_{INT} = 0, -100µA	*	4.1	4.3	4.5	V
HSNSPn, HSNSMn							
ΔV_{HSNS_ILIM}	Analog Foldback Current Limit Threshold	$\Delta V_{HSNS\_ILIMn} = (V_{HSNSPn}-V_{HSNSMn})$; $V_{IN}-V_{OUTPn}$ < 12V; V_{HSNSPn} = 6V, 60V	*	177	186	193	mV
		$V_{IN}-V_{OUTPn}$ = 60V; V_{HSNSPn} = 60V	*	37	41	46	mV
I_{IN_HSNSPn}	HSNSPn Input Current	$V_{IN} = V_{HSNSPn} = V_{HSNSMn}$ = 60V	*		95	190	µA
I_{IN_HSNSMn}	HSNSMn Input Current	$V_{IN} = V_{HSNSPn} = V_{HSNSMn}$ = 60V	*		66	128	µA
LSNS0							
ΔV_{LSNS_FCB0}	Port 0 Forward Circuit Breaker Threshold	$\Delta V_{LSNS\_FCB0} = (V_{OUTM0}-V_{LSNS0})$	*	60	76	90	mV
ΔV_{LSNS_RCB0}	Port 0 Reverse Circuit Breaker Threshold	$\Delta V_{LSNS\_RCB0} = (V_{LSNS0}-V_{OUTM0})$	*	60	76	90	mV
V_{SLP_RCB}	Deep Sleep Return Path Reverse Fault Threshold	All Ports in SLEEP/DISABLED State; Serial Bus Idle; $V_{SLP\_RCB} = V_{LSNS0}$	*	–1.2	–0.87	–0.25	V
I_{SLP_FCB}	Deep Sleep Return Path Forward Fault Threshold	All Ports in SLEEP/DISABLED State; Serial Bus Idle	*	15	34	45	mA
I_{SLP_LSNS0}	Deep Sleep Return Path Short Circuit Current	All Ports in SLEEP/DISABLED State; Serial Bus Idle; V_{LSNS0} = 2.5V	*	40	79	110	mA
R_{SLP_LSNS0}	Deep Sleep Return Path Impedance	All Ports in SLEEP/DISABLED State; Serial Bus Idle; I_{LSNS0} = 10mA	*	17	22	45	Ω
LSNS1/2, LSNS3/4							
ΔV_{LSNS_FCBn}	Forward Circuit Breaker Threshold	$\Delta V_{LSNS\_FCBn} = (V_{OUTMn}-V_{LSNSn})$	*	60	76	90	mV
ΔV_{LSNS_RCBn}	Reverse Circuit Breaker Threshold	$\Delta V_{LSNS\_RCBn} = (V_{LSNSn}-V_{OUTMn})$	*	60	76	90	mV
I_{LSNSn}	Input Current	V_{LSNSn} = –0.1V, 0.1V			–2.5		µA
HGATEn							
ΔV_{HGATEn}	External Port Source Path N-Channel MOSFET Gate Drive	AUTO High $\Delta V_{HGATEn} = (V_{HGATEn}-V_{OUTPn})$; I_{HGATEn} = 0, –1µA	*	9.3	10.2	10.6	V
I_{HGATE_UPn}	HGATEn Pull-Up Current	POWER_ON State; ΔV_{HGATEn} = 3V	*	–45	–34	–28	µA
I_{HGATE_FASTn}	HGATEn Fast Pull-Down Current	POWER_ON State; $V_{HSNSPn}-V_{HSNSMn}$ = 0.3V;ΔV_{HGATEn} = 3V	*	40	72	150	mA
I_{HGATE_SLOWn}	HGATEn Slow Pull-Down Current	DISABLED State; ΔV_{HGATEn} = 1.5V; V_{OUTPn} = 0V	*	8	16	24	mA
		DISABLED State; ΔV_{HGATEn} = 1.5V; V_{OUTPn} = –2V	*	40	110	185	µA
$V_{PULLDOWN\_FASTn}$	HGATEn Fast Pull-Down Dropout Voltage	POWER_ON State; V_{OUTPn} = 0V; I_{HGATEn} = 1mA; $V_{HSNSPn}-V_{HSNSMn}$ = 0.3V	*		1.1	1.4	V
$V_{PULLDOWN\_SLOWn}$	HGATEn Slow Pull-Down Dropout Voltage	DISABLED State; V_{OUTPn} = 0V; I_{HGATEn} = 10µA	*		0.14	0.3	V
dV_{HGATEn}/dt	HGATEn Inrush Slew Rate	POWER_UP State; $V_{HSNSPn}-V_{HSNSMn}$ < 30mV	*	14	16.5	19	V/ms
LGATE							
ΔV_{LGATE}	External Return Path N-Channel Gate Drive	POWER_ON State 6V < V_{IN} < 8.6V; I_{LGATE} = 0, –1µA	*	V_{IN} – 0.2		V_{IN}	V
		POWER_ON State	*	8.25	9.5	9.8	V

ELECTRICAL CHARACTERISTICS

Table 2.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
		V_{IN} ≥ 8.6V; I_{LGATEn} = 0, –1mA					
$I_{LGATE(UP)}$	LGATE Pull-Up Current	AUTO High; $V_{LGATE} – V_{LSRC}$ = 3V	*	–3.3	–2.2	–0.6	mA
$I_{LGATE(DWN)}$	LGATE Pull-Down Current	LGATE Disabled V_{LGATE} = 3V; V_{LSRC} = 0V	*	70	180	270	mA
$V_{LGATE(OFF)}$	LGATE Pull-Down Voltage	LGATE Disabled I_{LGATE} = 10µA; V_{LSRC} = 0V	*		0.6	1	V
AUTO							
V_{AUTO}	Input Threshold Voltage	V_{AUTO} Rising	*	1.15	1.205	1.25	V
	Input Hysteresis	V_{AUTO} Falling			11		mV
I_{AUTO}	Input Current	V_{AUTO} = 5.5V	*	–100		100	nA
		Positive Going Spike			28		µs
t_{SP_AUTO}	Pulse Width of Spike Suppressed	Negative Going Spike			7		µs
Port Source Current Readback ADC							
	Resolution	(Note 9)			11		Bits
	Full-Scale				204.8		mV
	Gain Error	$V_{HSNSPn} – V_{HSNSMn}$ < 200mV (Note 7)	*			±2.5	%
	Offset	Code 2048 Center (Note 7)	*	–250	–50	150	µV
	Integral Nonlinearity	(Note 7)	*			±1	LSB
	Conversion Time	(Note 8)	*	3.3	3.6	4	ms
V_{IN}, Port Output Voltage, and Port Return Current Readback ADC (Global ADC)							
	Resolution	(Note 9)			11		Bits
		$V_{OUTPn} – V_{OUTMn}$, V_{IN}; Low Gain			72.09		V
	Voltage Readback Full-Scale	$V_{OUTPn} – V_{OUTMn}$, V_{IN}; High Gain			36.04		V
	Current Readback Full-Scale	$V_{OUTMn} – V_{LSNSn}$			204.8		mV
	Full-Scale Gain Error				±2.5		%
	Offset	Code 2048 Center			±1		LSB
	Integral Nonlinearity				±1		LSB
	Conversion Time	(Note 8)	*	3.3	3.6	4	ms
Internal Check Voltage Reference (Accessible through the Global ADC)							
	Code				3548		LSB
	Tolerance		*			±3.5	%
	Conversion Time	(Note 8)	*	3.3	3.6	4	ms
Internal Temperature Sensor (Accessible through the Global ADC)							
	Weight				0.25		°C/LSB
	Error				±5		°C
	Conversion Time	(Note 8)	*	3.3	3.6	4	ms
SDI, SCK, $\overline{CS}$							
V_{ILD}	Digital Input Low Voltage		*			0.8	V
V_{IHD}	Digital Input High Voltage		*	2			V
I_{SPI}	Input Current	V_{SDI}, V_{SCK}, $V_{\overline{CS}}$ = 5.5V	*	–1		1	µA
SDO, SWn							
V_{OL}	Output Low Voltage	I_{SDO}, I_{SWn} = 3mA	*			0.4	V
I_{LEAK}	Output Leakage Current	V_{PIN} = 5.5V	*	–1		1	µA
Thermal Shutdown Internal Temperature							
$T_{SHUTDOWN}$	Thermal Shutdown Junction Temperature				175		°C
$T_{SHUTDOWN(HYST)}$	Thermal Shutdown Junction Temperature Hysteresis				30		°C

ELECTRICAL CHARACTERISTICS

Table 2.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OUTPn, OUTMn							
V_{OC}	Open-Circuit Detection Voltage	DETECTION State; I_{OUTPn} = 0	*	5.05	5.2	5.5	V
$V_{BAD\_HI\_PSE}$	Invalid PD Signature Voltage High-Range	DETECTION State; mr_valid_signature = FALSE	*	4.7		5	V
$V_{BAD\_LO\_PSE}$	Invalid PD Signature Voltage Low-Range	DETECTION State; mr_valid_signature = FALSE	*	3.7		4.05	V
V_{SLEEP}	SLEEP State Output Voltage	SLEEP State; I_{OUTPn} = 0, –1.85mA, 100µA	*	3.15	3.4	3.575	V
$V_{DISABLE}$	Port Disabled Voltage at OUTPn	Port Disabled; I_{OUTPn} = 50µA	*			1	V
$I_{DISCHARGE}$	OUTPn Discharge Current During SETTLE_SLEEP State	SETTLE_SLEEP State, I_{OUTPn},V_{OUTPn}-V_{OUTMn} = 6V	*	1.2	2.1	3.6	mA
I_{SC}	Short-Circuit Current	SLEEP State, I_{OUTPn}	*	–6.8	–5.5	–4.25	mA
I_{WAKEUP}	Valid Wakeup Current Input Range	SLEEP State, I_{OUTPn}	*	–1.85		-1.25	mA
I_{VALID}	Detection Probe Current range	DETECTION State, V_{OUTPn}-V_{OUTMn} = 0	*	–16	–14	–12	mA
		DETECTION State, V_{OUTPn}-V_{OUTMn} = 4.7V	*	–16	–13	–11	mA
ΔV_{OUTP_PWRGDn}	High-Side Power Good Threshold Voltage	Port Enabled; ΔV_{OUTP_PWRGDn} = V_{OUTPn}-V_{IN}; V_{OUTMn} = 0V; V_{OUTPn} Rising	*	390	440	510	mV
$\Delta V_{OUTP\_PWRGDn(HYST)}$	High-Side Power Good Threshold Voltage Hysteresis	Port Enabled; V_{OUTPn} Falling			22		mV
ΔV_{OUTM_PWRGDn}	Low-Side Power Good Threshold Voltage	Port Enabled; ΔV_{OUTMn_PWRGDn} = V_{OUTMn} ΔV_{OUTP_PWRGDn} = 0V	*	150	200	250	mV
WAKEUP							
I_{PU}	Internal Pull-Up Current	V_{WAKEUP} = 1.2V	*	–125	–100	–75	µA
R_{PD}	Internal Pull-Down Resistance	V_{WAKEUP} = 5.5V	*	0.4	1.2	2.25	MΩ
V_{OH}	Internal Pull-Up Voltage	I_{WAKEUP} = 0, 50µA	*	3.25	3.8	4.5	V
V_{ITH}	Input Threshold Voltage	V_{WAKEUP} Rising	*	1.15	1.205	1.25	V
$V_{ITH(HYST)}$	Input Threshold Voltage Hysteresis	V_{WAKEUP} Falling			10		mV
t_{SP_WAKEUP}	Pulse Width of Spike Suppressed	Positive Going Spike			30		µs
		Negative Going Spike			6		µs
Port Timing Characteristics							
t_{DET}	DETECTION State Timeout	DETECTION State; Invalid Signature	*	2.55		3.11	ms
t_{SIG_HOLD}	Detection Signature Hold Time	DETECTION State; Valid Signature	*	1		1.22	ms
t_{INRUSH_TOL}	POWER_UP State Timeout Tolerance	POWER_UP State; Short-Circuit; Programmable	*			±7	%
t_{LIM_TOL}	HSNS Overload Fault Delay Time Tolerance	Programmable; HSNS Circuit Breaker Threshold Exceeded	*			±7	%
t_{LSNS_FAULT}	LSNS Circuit Breaker Delay Time	V_{LSNSn} = 1.2V	*	1.3	1.8	2.4	µs
		V_{LSNSn} = –0.1V	*	2	4	6.3	µs
t_{OD_TOL}	OVERLOAD Delay Tolerance	OVERLOAD State; Programmable	*			±7	%
t_{MFVS}	MFVS Valid Hold Time	MFVS Present to mfvs_valid	*	4	5	6	ms
t_{MFVDO}	MFVS Dropout Time	MFVS Absent to tmfvdo_timer_done	*	300	350	400	ms
$t_{LIM\_SLEEP\_TOL}$	OUTPn Sleep Regulator Overload Fault Delay Time Tolerance	IDLE or SLEEP States; Programmable	*			±20	%
$t_{RESTART\_TOL}$	RESTART Delay Tolerance	RESTART State; Programmable	*			±7	%
t_{WAKEUP}	Wakeup Deglitch Time		*	0.05		0.1	ms
t_{OFF}	Turn Off Time	SETTLE_SLEEP to OVERLOAD; V_{OUTPn} = 5V	*	409		500	ms
SPI Bus Timing							
f_{CLK}	SCK Frequency		*			1	MHz
t_1	SDI Setup Time Before SCK Rising Edge		*	26			ns
t_2	SDI Hold Time After SCK Rising Edge		*	25			ns
t_3	SCK Low		*	200			ns
t_4	SCK High		*	200			ns

ELECTRICAL CHARACTERISTICS

Table 2.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_5	$\overline{CS}$ Rising Edge to $\overline{CS}$ Falling Edge		*	650			ns
t_6	SCK Rising Edge to $\overline{CS}$ Rising Edge		*	800			ns
t_7	$\overline{CS}$ Falling Edge to SCK Rising		*	1			µs
t_8	SCK Falling Edge to SDO Valid	(Note 6)	*			100	ns
t_9	$\overline{CS}$ Rising Edge to SDO Rising	(Note 6)	*			250	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: This IC includes over-temperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: Externally forced voltage absolute maximums. The LTC4296-1 may exceed these during normal operation.

Note 5: The LTC4296-1 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4296-1A is guaranteed over the –40°C to 125°C operating junction temperature range.

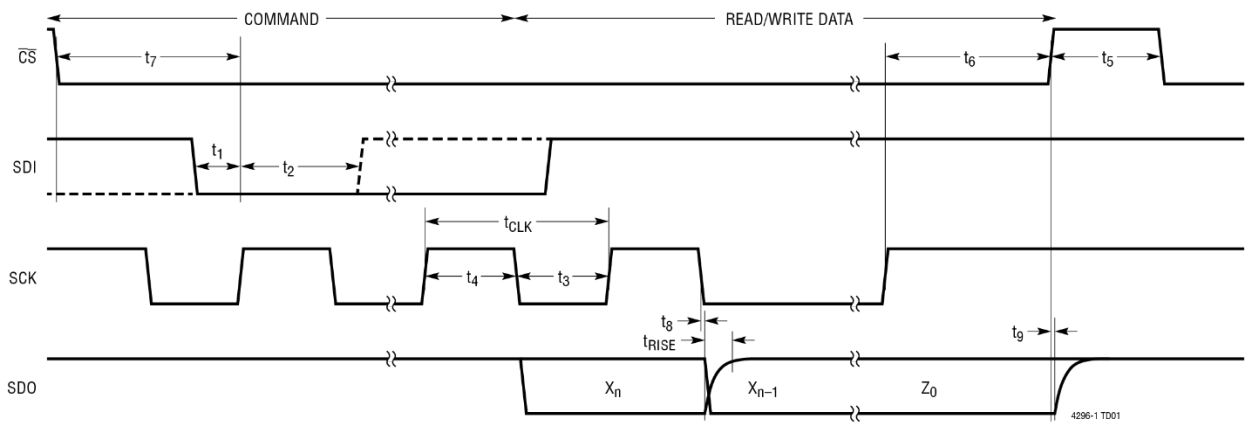
Note 6: These specifications do not include the rise or fall time of SDO. While fall time (typically 5ns due to the internal pull-down transistor) is not a concern, rising-edge transition time t_{RISE} is dependent on the pull-up resistance and load capacitance on the SDO pin.

Note 7: These specifications are tested at V_{IN} = 6V. The operation at V_{IN} = 60V is guaranteed by design.

Note 8: These specifications are guaranteed by design.

Note 9: Both port and global ADCs have a bipolar input range which is spanned by 11-bits plus a sign bit.

SPI BUS TIMING DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

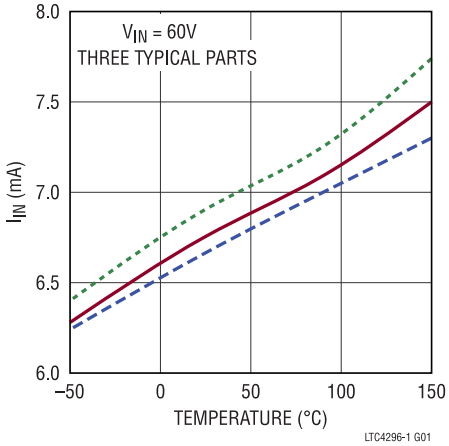


Figure 2. I_{IN} vs. Temperature, All Ports in POWER_ON State

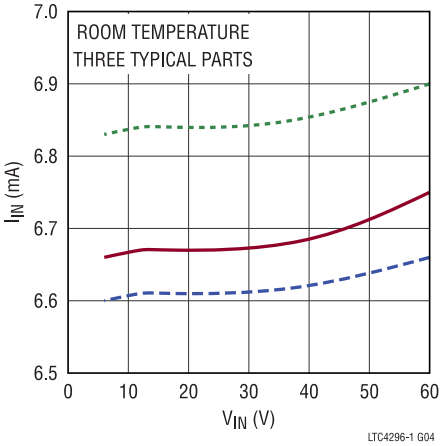


Figure 5. I_{IN} vs. V_{IN}, All Ports in POWER_ON State

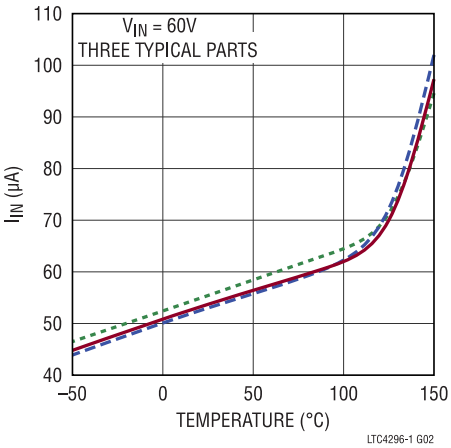


Figure 3. I_{IN} vs. Temperature, All Ports in SLEEP State

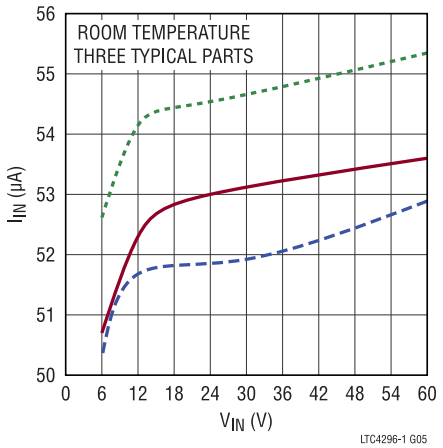


Figure 6. I_{IN} vs. V_{IN}, All Ports in SLEEP State

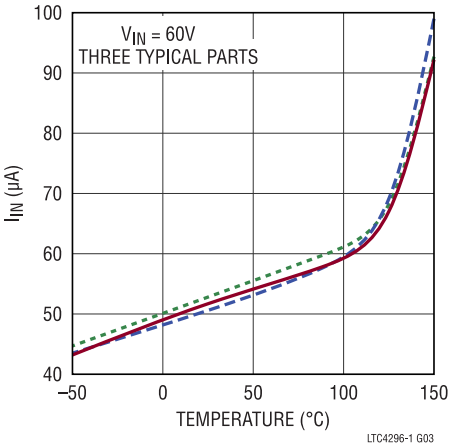


Figure 4. I_{IN} vs. Temperature, All Ports in DISABLED State

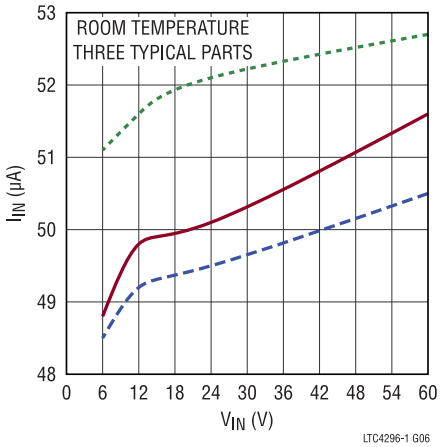


Figure 7. I_{IN} vs. V_{IN}, All Ports in DISABLED State

TYPICAL PERFORMANCE CHARACTERISTICS

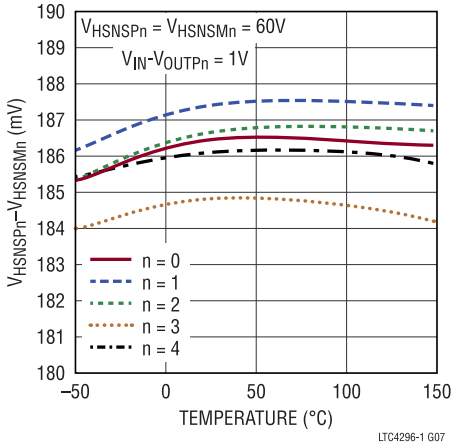


Figure 8. Analog Foldback Current Limit Threshold vs. Temperature

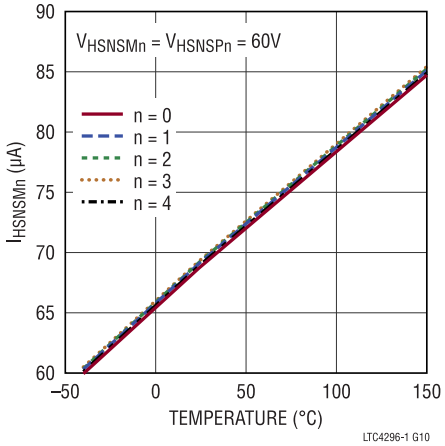


Figure 11. I_{HSNSMn} vs. Temperature, Port in POWER_ON State

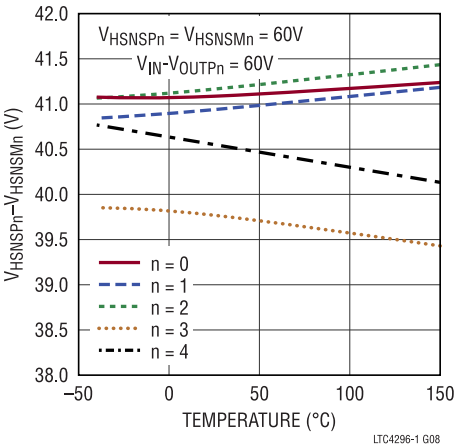


Figure 9. Analog Foldback Current Limit Threshold vs. Temperature

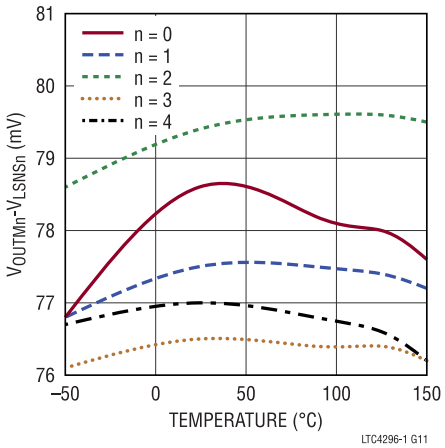


Figure 12. LGATE Circuit Breaker Threshold vs. Temperature

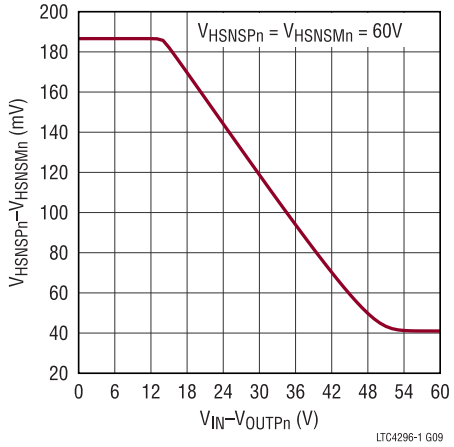


Figure 10. Analog Foldback Current Limit Threshold Voltage vs. V_{IN}-V_{OUTPn}

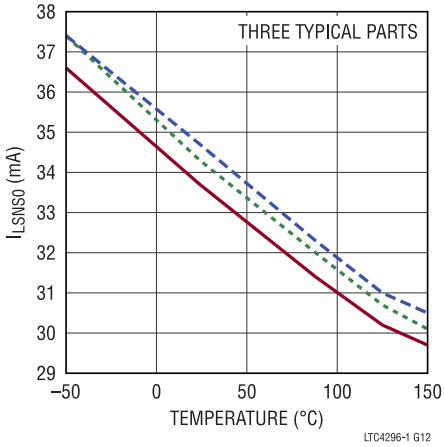


Figure 13. Deep Sleep Return Path Forward Fault Threshold vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

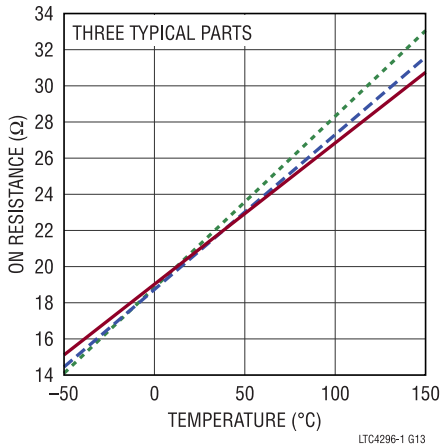


Figure 14. Deep Sleep Return Path On Resistance vs. Temperature

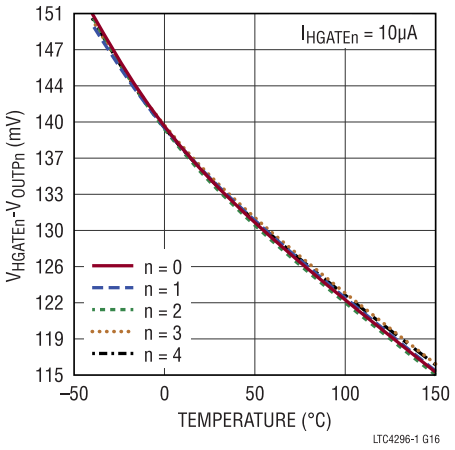


Figure 17. HGATEn Slow Pull-Down Dropout Voltage vs. Temperature

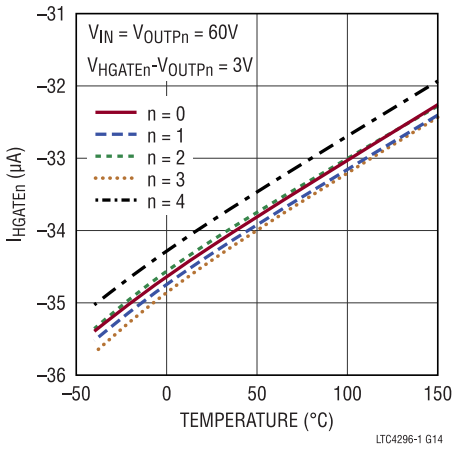


Figure 15. HGATEn Pull-Up Current vs. Temperature

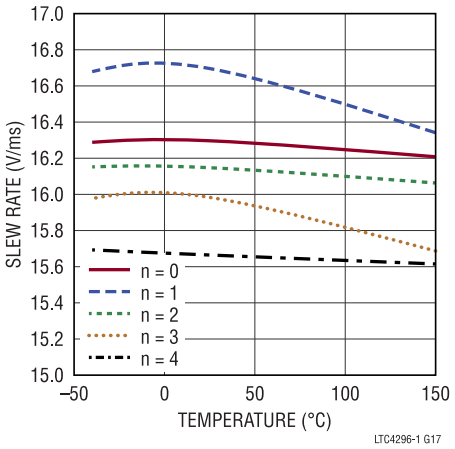


Figure 18. HGATEn Inrush Slew Rate vs. Temperature

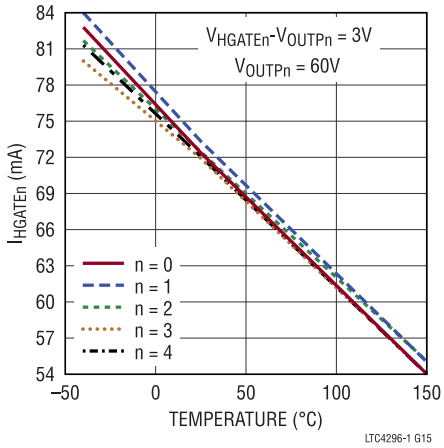


Figure 16. HGATEn Fast Pull-Down Current vs. Temperature

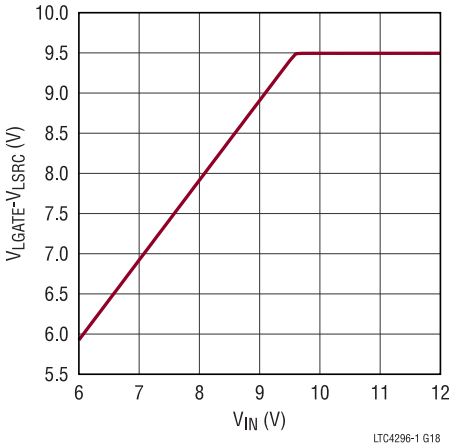


Figure 19. Low-Side N-Channel GATE Drive vs. V_{IN}

TYPICAL PERFORMANCE CHARACTERISTICS

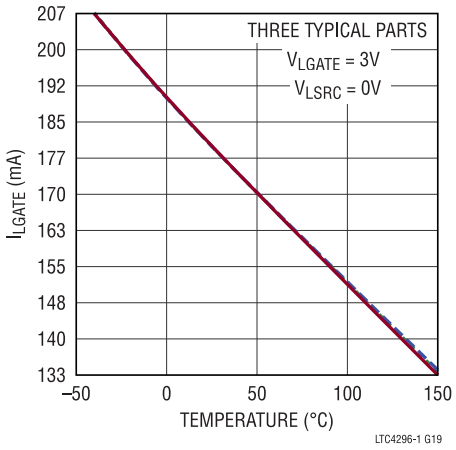


Figure 20. LGATE Pull-Down Current vs. Temperature, LGATE Disabled

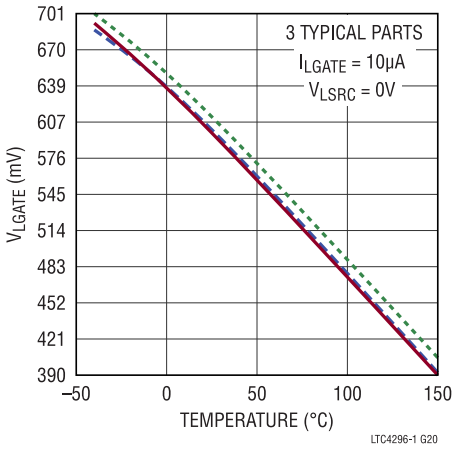


Figure 21. LGATE Pull-Down Voltage vs. Temperature

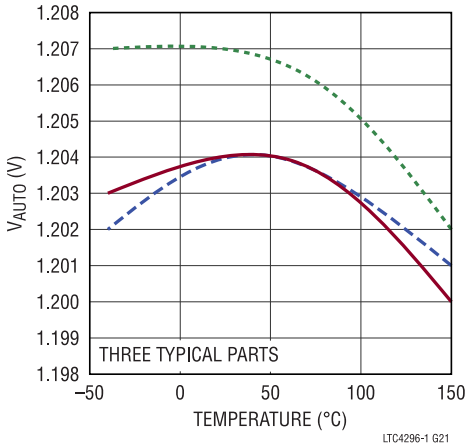


Figure 22. AUTO Input Threshold Voltage vs. Temperature, Rising-Edge

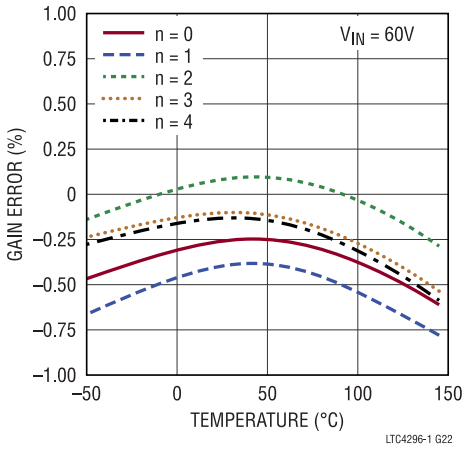


Figure 23. Port ADC Gain Error vs. Temperature

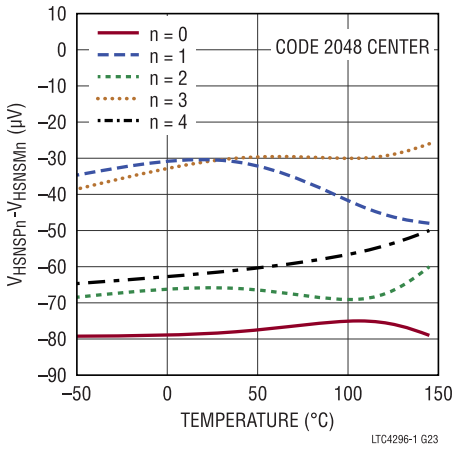


Figure 24. Port ADC Offset vs. Temperature

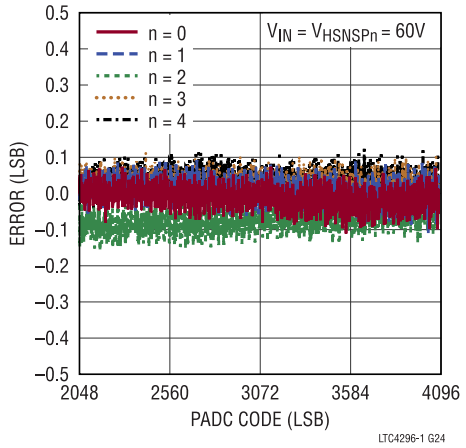


Figure 25. Port ADC INL

TYPICAL PERFORMANCE CHARACTERISTICS

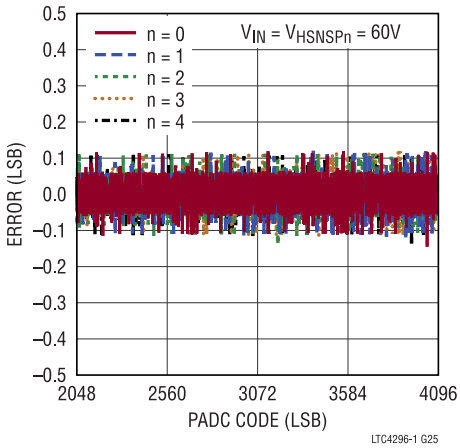


Figure 26. Port ADC DNL

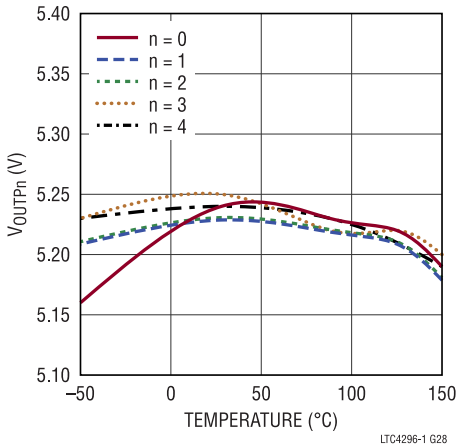


Figure 29. Open-Circuit Detection Voltage vs. Temperature

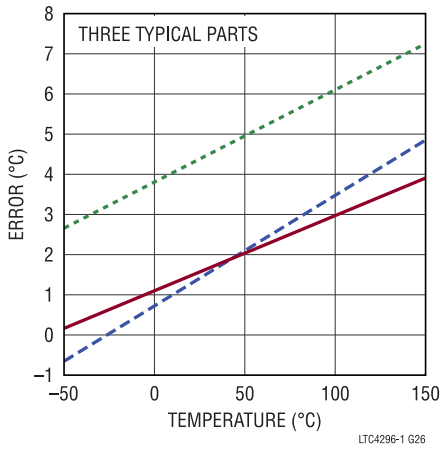


Figure 27. Internal Temperature Sensor Error vs. Temperature

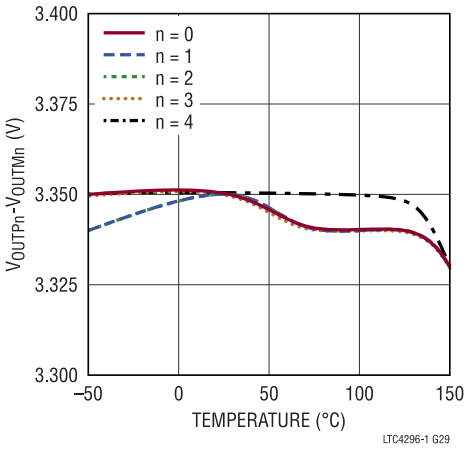


Figure 30. SLEEP State Open-Circuit Output Voltage vs. Temperature

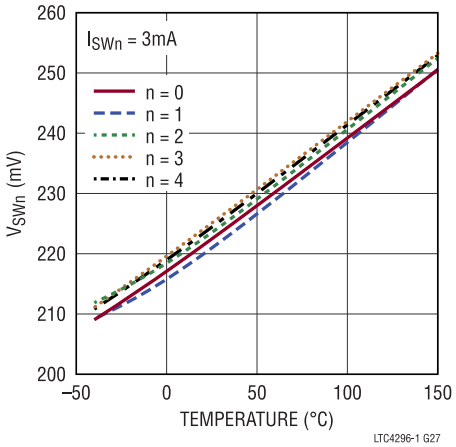


Figure 28. SWn Low Output Voltage vs. Temperature

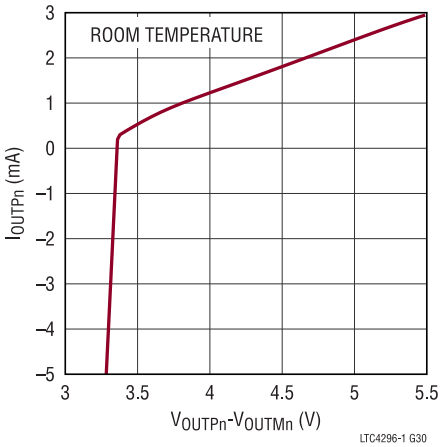


Figure 31. I_{OUTPn} vs. V_{SLEEP}

TYPICAL PERFORMANCE CHARACTERISTICS

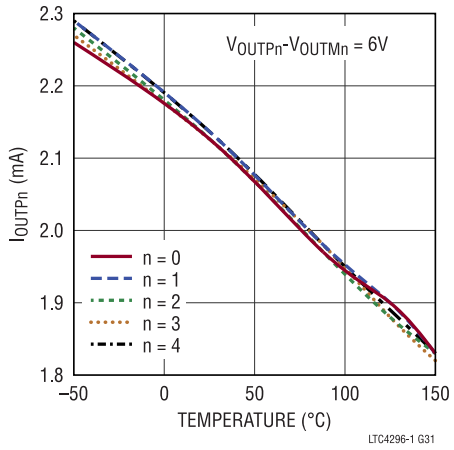


Figure 32. $I_{DISCHARGE}$ vs. Temperature

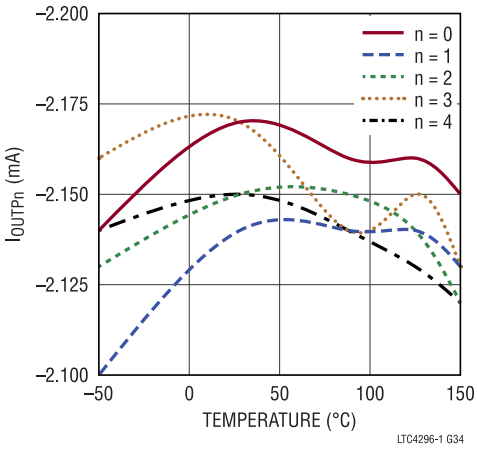


Figure 35. Valid Wakeup Current High Threshold vs. Temperature

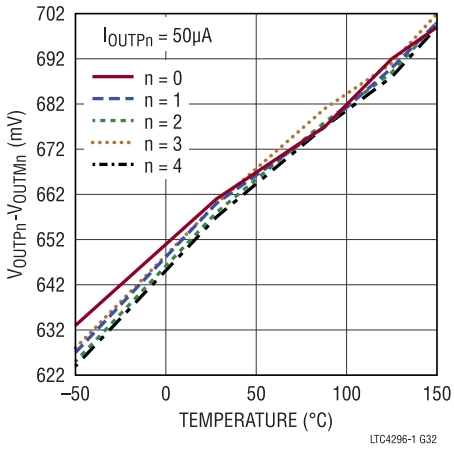


Figure 33. $V_{DISABLE}$ vs. Temperature

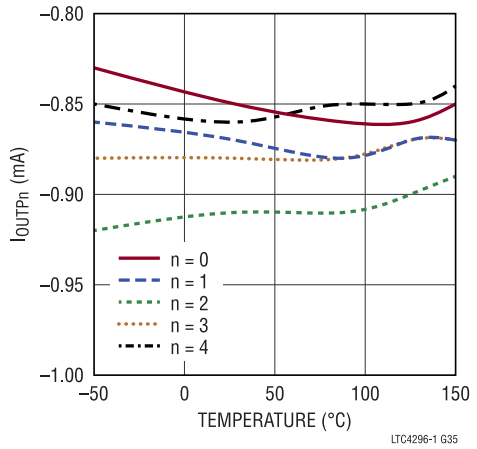


Figure 36. Valid Wakeup Current Low Threshold vs. Temperature

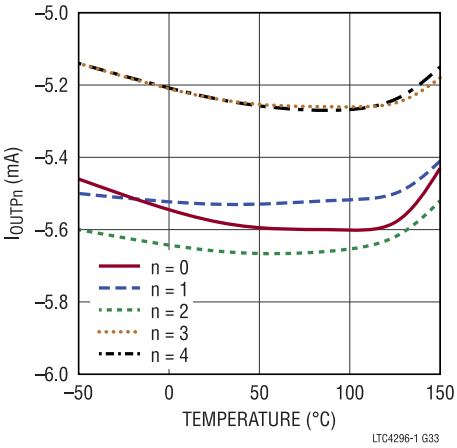


Figure 34. Short-Circuit I_{OUTPn} vs. Temperature, SLEEP State

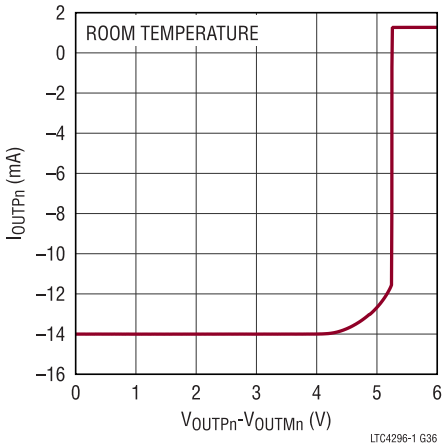


Figure 37. I_{VALID} vs. V_{OUTPn}-V_{OUTMn}

TYPICAL PERFORMANCE CHARACTERISTICS

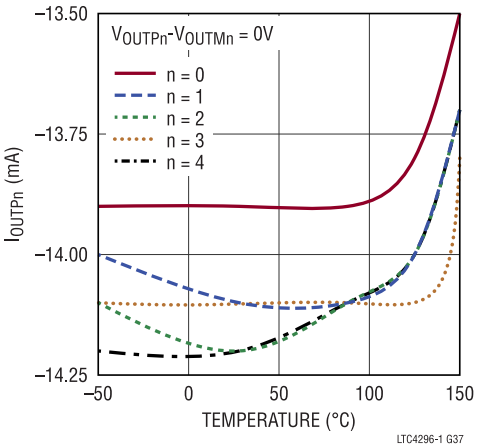


Figure 38. I_{VALID} vs. Temperature

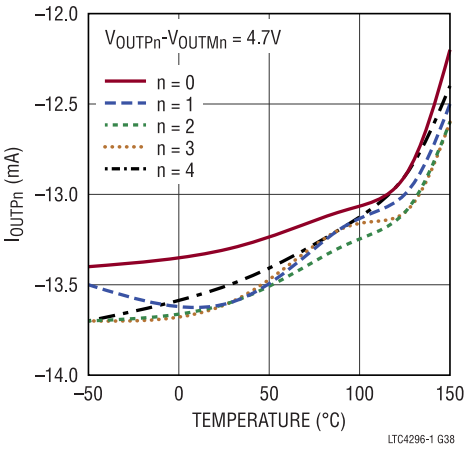


Figure 39. I_{VALID} vs. Temperature

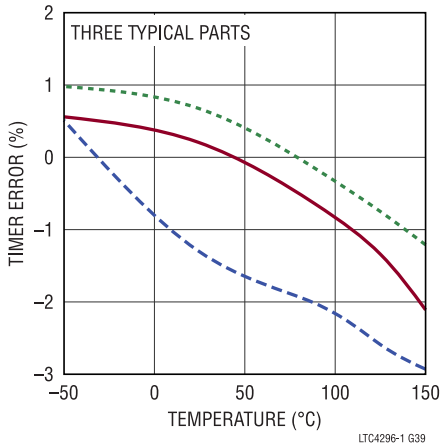


Figure 40. Timer Error vs. Temperature, IDLE, DETECTION/CLASSIFICATION, or POWER_ON States

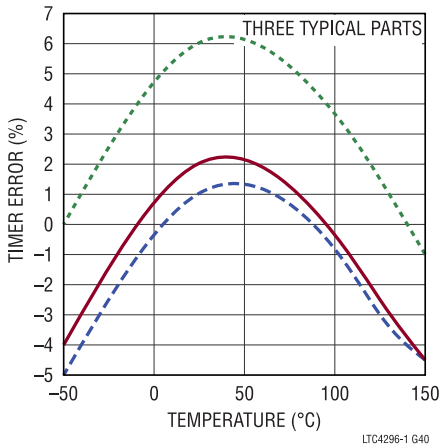


Figure 41. Timer Error vs. Temperature, All Ports DISABLED, or SLEEP States

PIN FUNCTIONS

Pin No.	Mnemonic	Description
Pins 1, 33, 37, 41, 45	OUTPn	Portn Positive Output. Connect to source of port n top-side external N-channel MOSFET. Do not connect if port n is unused.
Pins 2, 34, 38, 42, 46	HGATEn	Portn High-Side Gate Drive. Connect to gate of port n top-side external N-channel MOSFET. Do not connect if port n is unused.
Pins 3, 35, 39, 43, 47	HSNSMn	Portn High-Side Kelvin Sense Negative Input. Connect directly to the negative terminal of port n top-side current sense resistor. Connect the sense resistor negative terminal to the drain of port n top-side external N-channel MOSFET. If port n is unused, connect to HSNSPn.
Pins 4, 36, 40, 44, 48	HSNSPn	Portn High-Side Kelvin Sense Positive Input. Connect directly to the positive terminal of port n top-side current sense resistor. If port n is unused, connect to IN.
Pin 23	LGATE	Low-Side Gate Drive. If a low-side external N-channel MOSFET is present, connect to the MOSFET gate. Do not connect if a low-side external MOSFET is not present.
Pin 24	LSRC	Low-Side External MOSFET Source Connection. Connect to GND.
Pin 25	OUTM0	Port 0 Negative Output and Low-Side Kelvin Sense Positive Input. Connect directly to the positive terminal of port 0 low-side current sense resistor. Connect to LSNS0 if port 0 is unused.
Pin 26	LSNS0	Port 0 Low-Side Kelvin Sense Negative Input. Connect directly to the negative terminal of port 0 low-side current sense resistor. If a low-side external N-channel MOSFET is present, connect to the MOSFET drain. If a low-side external MOSFET is not present, connect to GND.
Pin 27	OUTM1	Port 1 Negative Output and Low-Side Kelvin Sense Positive Input. Connect directly to the positive terminal of port 1 low-side current sense resistor. Connect to LSNS1/2 if port 1 is unused.
Pin 28	LSNS1/2	Ports 1 and 2 Low-Side Kelvin Sense Negative Input. Connect directly to the negative terminals of port 0 and port 1 low-side current sense resistors. If a low-side external N-channel MOSFET is present, connect to the MOSFET drain. If a low-side external MOSFET is not present, connect to GND.
Pin 29	OUTM2	Port 2 Negative Output and Low-Side Kelvin Sense Positive Input. Connect directly to the positive terminal of port 2 low-side current sense resistor. Connect to LSNS1/2 if port 2 is unused.
Pin 30	OUTM3	Port 3 Negative Output and Low-Side Kelvin Sense Positive Input. Connect directly to the positive terminal of port 3 low-side current sense resistor. Connect to LSNS3/4 if port 3 is unused.
Pin 31	LSNS3/4	Ports 3 and 4 Low-Side Kelvin Sense Negative Input. Connect directly to the negative terminals of port 3 and port 4 low-side current sense resistors. If a low-side external N-channel MOSFET is present, connect to the MOSFET drain. If a low-side external MOSFET is not present, connect to GND.
Pin 32	OUTM4	Port 4 Negative Output and Low-Side Kelvin Sense Positive Input. Connect directly to the positive terminal

PIN FUNCTIONS

Pin No.	Mnemonic	Description
		of port 4 low-side current sense resistor. Connect to LSNS3/4 if port 4 is unused.
Pin 6	IN	Supply Voltage Input.
Pin 7	CPO	Charge Pump Output. Connect a 1nF, 16V capacitor from CPO to IN.
Pin 8	INT	Internal 4.3V Regulator Bypass. Connect a 470nF bypass capacitor from INT to GND.
Pin 9	SDI	SPI Serial Data Input.
Pin 10	SDO	SPI Serial Data Open-Drain Output. Connect to logic high through a pull-up resistor.
Pin 11	SCK	SPI Serial Clock Input.
Pin 12	$\overline{CS}$	SPI Chip Select Input, Active Low.
Pin 13	AUTO	Auto Mode Enable for All Ports, Active High. Tie AUTO low to configure LTC4296-1 in manual mode for performing microcontroller assisted PD Classification. Tie AUTO high for applications that support physical detection. See Autonomous Mode section section for additional usage of the AUTO pin.
Pin 14	WAKEUP	Bidirectional Wakeup. During a PD initiated wakeup event on a port, the pin is pulled high to 3.75V with an internal 100µA pull-up current. The pin is pulled down to GND by an internal 1.2MΩ resistor. The pin may also be pulled to logic high externally, to wake up one or more ports. Do not connect if unused.
Pins 16, 17, 18, 19, 20	SWn	Open-Drain Snubber Switch Output for Portn, Active High. Drives an external N-channel MOSFET to disconnect the power snubber during classifcation. See Classification section. Do not connect if unused.
Pin 22	RT	Connect a 24.3kΩ resistor between RT and GND to set the internal oscillator frequency.
Pin 5, 15	DNC	Do Not Connect. Must be left unconnected.
Pin 21	GND	Device Ground.
Pin 49	GND	Exposed Pad and Device Ground. Must be soldered to PCB ground.

OPERATION

OVERVIEW

The LTC4296-1 is the world's first IEEE 802.3cg, Single-pair Power over Ethernet (SPoE) compliant Power Sourcing Equipment (PSE) controller. It controls and monitors power delivery for up to five Powered Devices (PDs). The complementary data protocol for SPoE is 10BASE-T1L.

With a host microcontroller, the LTC4296-1 provides the circuitry needed to implement an IEEE 802.3cg compliant PSE design. Additional required components include per port external, N-channel MOSFET and sense resistor to implement high-side electronic circuit breakers with foldback analog current limit. An optional low-side N-channel MOSFET, combined with per port low-side sense resistors can be used to implement a low-side electronic circuit breaker. The LTC4296-1 application circuit provides fault-tolerance mandated by IEEE 802.3cg, increases system reliability, and minimizes power losses compared to designs with onboard MOSFETs.

The source and return circuit breakers offer protection against the following output faults at the connector:

- Short between the two conductors
- Short of one or both conductor(s) to an external positive voltage
- Short of positive conductor to ground

The host microcontroller is used to configure the LTC4296-1 for PD classification by writing to the configuration registers using the Serial Peripheral Interface (SPI). The host microcontroller may also communicate with the LTC4296-1 via SPI to read telemetry such as port status, port voltages and currents, etc. The data integrity of the SPI is verified with the Packet Error Checking (PEC) feature.

Single-pair Power Over Ethernet (SPoE)

SPoE is a standard protocol for sending power over two-wire Ethernet data cables. SPoE is similar in concept to traditional Power over Ethernet (PoE) but differs significantly in definition and implementation. The differences stem mainly from the unique power coupling techniques used in a two-wire circuit, as opposed to PoE's 4- and 8-wire, pair-oriented powering techniques. SPoE enables the simultaneous transmission of power and data over a single conductor pair, e.g., balanced twisted pair or coaxial cable (Figure 42).

Single pair Ethernet (SPE) data connections consist of a single pair of wires, AC coupled at each end to avoid ground loops. Unlike PoE systems that transmit power common mode to the data, SPoE systems diplex power and data over a single pair of conductors.

IEEE 802.3cg (SPoE) is an extension of 802.3bu Power over Data Lines (PoDL). The IEEE Standards Association ratified PoDL in 2016. Multiple complementary data standards are already ratified or in development, ranging from 10Mbps to 10Gbps and higher. PoDL defines protocols for detecting, classifying, powering, disconnecting, and standby power operation. IEEE 802.3cg was ratified in 2019 to add features targeting long reach protocols, such as 10BASE-T1L, with cable lengths of up to 1km.

SPoE was tailored to meet building and factory automation market requirements. It also defines the classification based power delivery protocol for the PSE and PD. Classification ensures PSE-PD compatibility and avoids applying power into a short or open circuit. The PSE performs detection, followed by classification, of the PD before applying full operating voltage. During classification the PSE requests information such as Class, Type, and Cable Resistance Measurement (CRM) support from the PD.

If the PSE determines the PD is compatible, it applies full operating voltage to the PD. If CRM is supported, the PSE and PD may negotiate allocation of surplus power to the PD. The PSE may skip classification and power up a PD that provides a valid detection signature. A PD providing an invalid detection signature, however, must undergo classification before being powered. A PD is required to present a valid MFVS to remain fully powered. If the PD is disconnected or goes to sleep, the PSE detects the absence of MFVS and removes full operating voltage. The PSE removes the output voltage entirely in the event of a fault or short circuit.

After removing the full operating voltage in the absence of MFVS, the PSE enters a low power sleep and provides V_{SLEEP} (3.3V typ) at the port.

Wakeup functions from sleep are flexible and can flow either upstream (PD initiated) or downstream (PSE initiated). The PD can request restoration of full operating voltage by presenting a wakeup current signature to the PSE. The PSE can also initiate a wakeup of the PD by providing full operating voltage after successful classification.

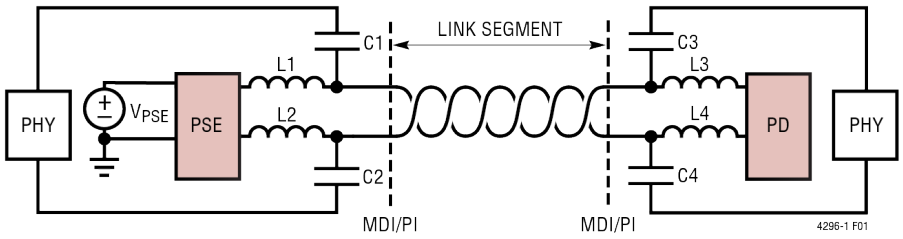


Figure 42. Basic SPoE Architecture

OPERATION

Table 3. IEEE 802.3cg Class Power Requirements Matrix for PSE and PD, and Example Link Segment Maximum Distances.

Class	Description	10	11	12	13	14	15
V_{PSE}(V)	PSE output voltage	20-30			50-58		
$I_{PI(max)}$(mA)	Cable current	92	240	632	231	600	1579
$P_{CLASS(min)}$(W)	PSE output power	1.85	4.8	12.63	11.54	30	79
$V_{PD(min)}$(V)	PD input voltage	14			35		
$P_{PD(max)}$(W)	PD power	1.23	3.2	8.4	7.7	20	52
$R_{LINK\_SEG\_LOOP}$(Ω)	Cable resistance	65	25	9.5	65	25	9.5
Example Cable		**Maximum Lengths (m)**					
14AWG	14 gauge cable	1000*	1000	400	1000*	1000	400
18AWG	18 gauge cable	1000	400	158	1000	400	158
24AWG	24 gauge cable	300	100	40	300	100	40

*IEEE 802.3cg limits cable length to 1000m

10BASE-T1L Field Switch PSE

The LTC4296-1 provides a solution for 10BASE-T1L field switches that require a PSE at each port.

Classification of the PD connected to each link segment ensures that the overall power provided to the switch is appropriately distributed across the sub-systems.

An example of a 10BASE-T1L field switch is shown in Figure 43. The field switch host processor manages the 5x port Ethernet switch (Integrated MAC) and the LTC4296-1 over a SPI interface.

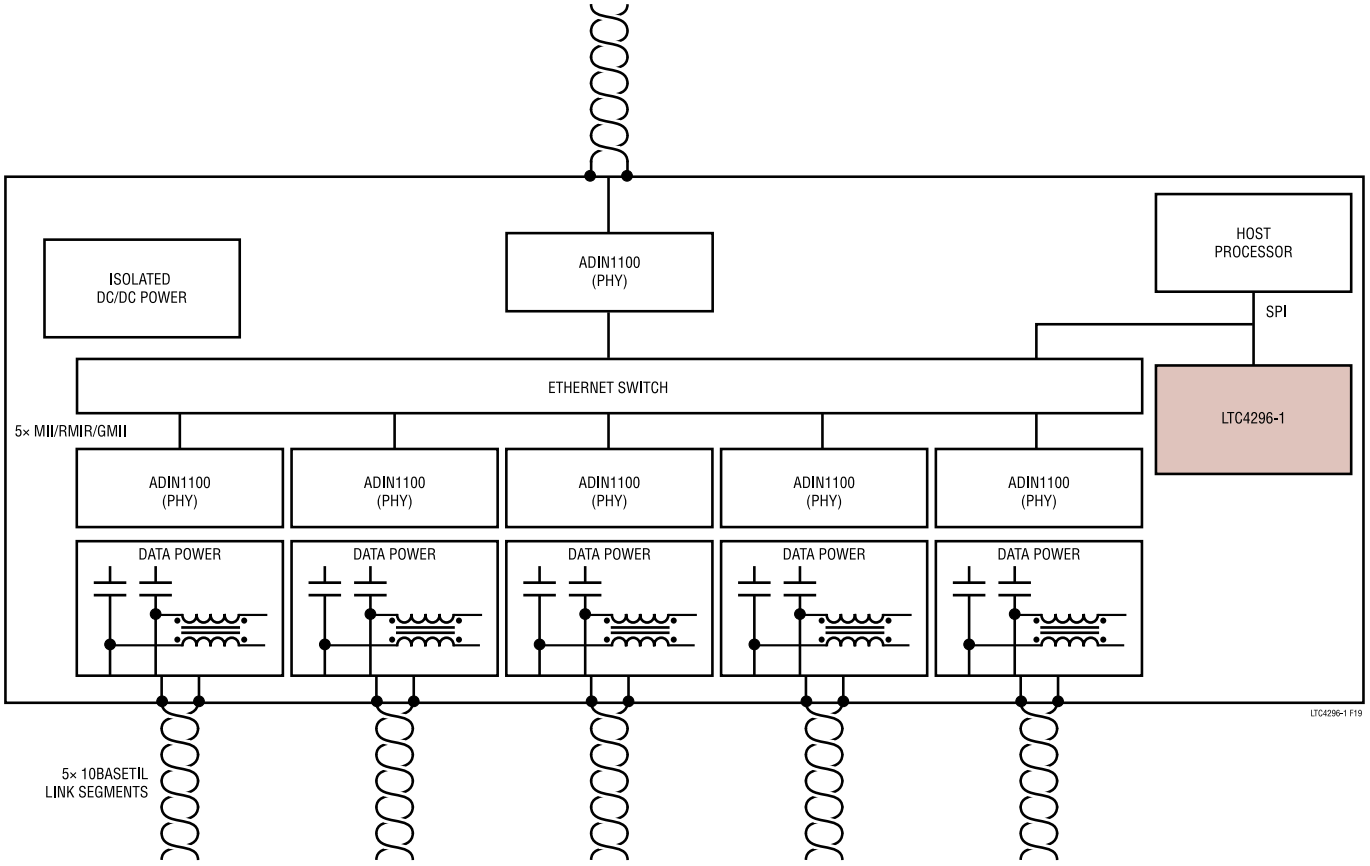


Figure 43. 10BASE-T1L PSE FIELD SWITCH

OPERATION

Classification for Discoverable Systems

SPoE Class defines the PSE output voltage range and maximum power being sourced or consumed in the system. PoDL comprises of Class 0 through 15. Class 10 through 15 are defined by IEEE 802.3cg for discoverable systems as shown in Table 3. Class 10 through 12 provide a 24V nominal PSE output voltage, as required by many industrial, factory automation, legacy building automation and "wet locations." Each of the three 24V classes represents a different cabling definition and accompanying maximum power transfer. Class 13 through 15 provide a 54V nominal PSE output voltage, to maximize power transfer without exceeding Safety Extra Low Voltage (SELV). Compatible SPoE PSE-PD Class pairs are shown in Table 4.

Table 4. PSE and PD Class Compatibility Matrix

		PSE Class					
		10	**11**	**12**	**13**	**14**	**15**
PD Class	**10**	Yes	Yes	Yes	No	No	No
	11	No	Yes	Yes	No	No	No
	12	No	No	Yes	No	No	No
	13	No	No	No	Yes	Yes	Yes
	14	No	No	No	No	Yes	Yes
	15	No	No	No	No	No	Yes

PoDL defines the Serial Communications Classification Protocol (SCCP) for classifying a PD. The SCCP uses three basic symbols: Initialization, Read-Slot, and Write-Slot. Application Note "Host Assisted SCCP with the LTC4296-1" provides a detailed description of SCCP.

IEEE 802.3cg also supports an optional CRM feature as part of SCCP. CRM allows a PSE to allocate additional power otherwise allocated for cable loss to a PD when connected through less than maximum allowed cable resistance.

DATA SHEET FONTS

The register and bit names in this data sheet are referred to using **bold faced** font. The example below explains the conventions used to refer to the registers and their field.

- **gfltst** refers to Global Fault Status register (Address 0x01h)
- **gfltev.command_fault** refers to the Command Fault Bit (bit 3 at 0x02h) in the Global Fault Event register
- Families of registers or bits for individual ports are referred to with an bold faced italic "*n*" and the addresses for the same are referred to with an italic "*m*", where *m* = *n* + 1. For example, p0st refers to the Port 0 Status register (address 0x12h) and p*n*st refers to Port*n* Status register (address 0x*m*2h) where *n* takes values from 0 to 4.

USAGE CASES

802.3cg PSE

The primary usage case for the LTC4296-1 is an 802.3cg compliant PSE. Here, the LTC4296-1 AUTO pin is pulled low and a host operates the LTC4296-1 ports semi-manually through the states shown in Figure 44. In each state, the LTC4296-1 will control the port output voltage accordingly.

From a system power up or device reset, the LTC4296-1 starts in the DISABLED state. An LTC4296-1 port is enabled by the host and moves on to the IDLE state. It then awaits a command from the host to move on to the next state.

OPERATION

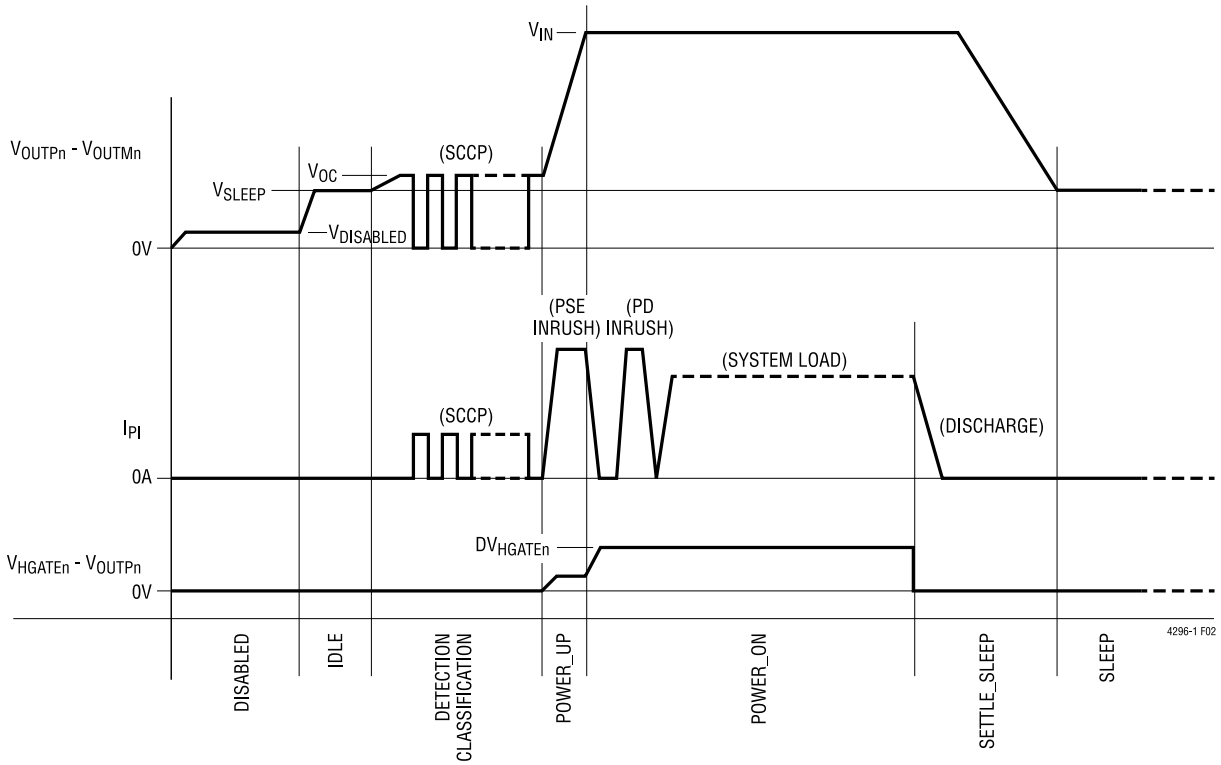


Figure 44. Simplified 802.3cg PSE State Sequence (Not to Scale)

When ready, the host configures the LTC4296-1 port to enter the DETECTION state; the LTC4296-1 checks the port current status before moving on to DETECTION.

When the port is in the DETECTION state, the host sets the LTC42961-1 to the CLASSIFICATION state and performs SCCP with a valid PD. Once the host micro-controller has determined the PD's Class is compatible, it may then command the port to enter the POWER_UP state.

During the POWER_UP state, the LTC4296-1 controls inrush and monitors the port output voltage to determine when inrush is complete.

After a successful power up, the port enters the POWER_ON state and remains there until the LTC4296-1 detects a current overload fault or an MFVS timeout, or is instructed by the host to exit POWER_ON when power is no longer available.

If the LTC4296-1 removes power to the port due to invalid MFVS, it will monitor the port voltage discharge in the SETTLE_SLEEP state.

The LTC4296-1 enters the low power SLEEP state after a successful port discharge. Here the LTC4296-1 waits for the user, host or PD to initiate a wakeup before returning to the DETECTION state.

While in the IDLE, POWER_ON, SETTLE_SLEEP or SLEEP state, the LTC4296-1monitors the port for current overload fault conditions. If one occurs, the LTC4296-1 will turn off the port and wait a set time in the OVERLOAD state before entering the IDLE state.

A port which fails to exit either the DETECTION or POWER_UP states successfully before the maximum allotted time will enter the RESTART state. It then waits a set time before re-entering the IDLE state.

Autonomous Mode

For applications that do not require classification, the LTC4296-1 can operate in an autonomous mode without a host controller with the AUTO pin pulled high. In autonomous mode, the LTC4296-1 will power up any port when a PD presents a valid detection signature. This mode is ideal for applications that only require a basic detection. Power up can be forced regardless of the detection signature by setting the signature override good bit (**pncfg1.sig_override_good**).

PORT STATE DESCRIPTIONS

Overview

Every port in the LTC4296-1 implements the PSE state described in the Usage Cases. A detailed description of each state is provided in the subsequent sections.

OPERATION

DISABLED State

A port starts in the DISABLED state after a power on or software reset event. In this state, the high-side MOSFET is turned off and the port voltage is discharged to less then $V_{DISABLED}$ with an internal pull-down. The port remains here until it is enabled by the software enable bit (***pn*cfg0.sw_en**) or if the AUTO pin is high and not masked (***pn*cfg0.hw_en_mask**). Once enabled, the port enters the IDLE state.

IDLE State

In the IDLE state, the port output is biased by the LTC4296-1 to V_{SLEEP}. If the output voltage is in the range of V_{SLEEP}, output current is less than $I_{WAKEUP(max)}$, and the AUTO pin is high or Software PSE Ready is asserted (***pn*cfg0.sw_pse_ready**), the port proceeds to the DETECTION state. If the port current exceeds I_{WAKEUP} for t_{LIM_SLEEP} the port will enter the OVERLOAD state.

DETECTION State

PD detection is performed in the DETECTION state. During detection a probing current, I_{VALID}, is sourced and the port searches for a PD. A PD not requiring classification presents a voltage in the range of V_{GOOD_PSE} when the PSE applies the probing current.

A PSE must accept voltages as valid in the range of V_{GOOD_PSE} for at least t_{SIG_HOLD} and must reject voltages less than $V_{BAD\_LO\_PSE}$ or greater than $V_{BAD\_HI\_PSE}$ (dark shaded regions in Figure 46). A PSE may accept or reject voltages in the undefined ranges between the must-reject and must-accept limits (light shaded regions).

A port will exit the DETECTION state after t_{DET} unless the detection timer is disabled (***pn*cfg0.tdet_disable**). If the t_{DET} timer expires without detecting a valid PD, the port enters the RESTART state and then returns to IDLE. Figure 45 shows a typical valid PD detection sequence.

For use cases not requiring classification, the following conditions need to be met to proceed to POWER_UP:

A valid detection signature is found (or the ***pn*cfg1.sig_override_good** bit is set).

The Global Software Power Good bit is set (**gcfg.sw_vin_pgood**).

The Port Software Power Available bit is set (***pn*cfg0.sw_power_available**)

If the Port Software Power Available bit is not set, the port goes to the RESTART state after exiting the DETECTION state.

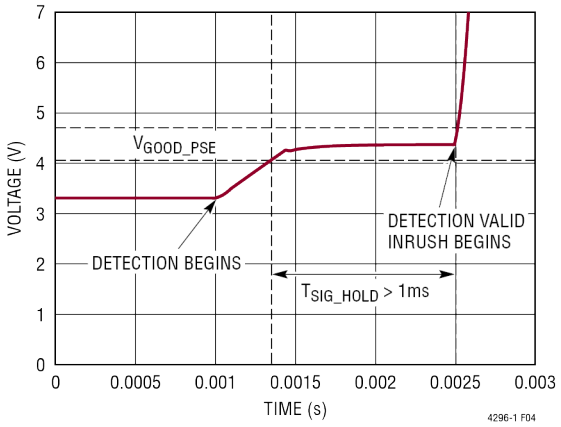


Figure 45. Typical Valid Detection Sequence Waveform

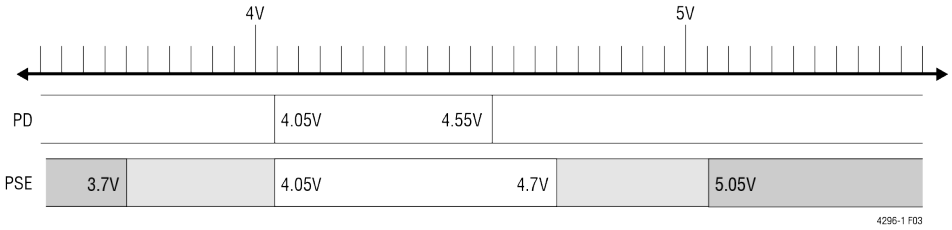


Figure 46. IEEE 802.3bu Signature Voltage Range

OPERATION

CLASSIFICATION State

Classification is performed in the DETECTION state by the host microcontroller using SCCP. Please refer to Application Note “Serial Communication Classification Protocol for 5-Port SPoE PSE Controller LTC4296-1” for a detailed description of how to implement SCCP with the host microcontroller.

Classification is configured by setting the Software PSE Ready bit (**p*n*cfg0.sw_pse_ready**) and setting the Classification Mode bit (**p*n*cfg0.set_classification_mode**) prior to entering the DETECTION state. When the Classification Mode bit is asserted while in the DETECTION state, the port SWn pin pulls low to disable the external port snubber switch MOSFET (M2).

If the microcontroller determines a valid PD with a compatible Class is present, the port can proceed to the POWER_UP state by setting Port Software Power Available (**p*n*cfg0.sw_power_available**) and End_classification (**p*n*cfg0.end_classification**).

If a PD with a valid signature or a PD with compatible Class is not present, the port can be returned to the IDLE state via the RESTART state by clearing Port Software Power Available and setting **p*n*cfg0.end_classification**.

POWER_UP State

In the POWER_UP state, the port ramps up the HGATEn voltage in a controlled manner to limit inrush current. Under normal power up circumstances, the HGATEn voltage will increase until the port reaches the current sense resistor voltage limit, ΔV_{HSNS_ILIM}, or until the maximum HGATEn slew-rate, dV_{HGATEn}/dt is reached. The t_{INRUSH} timer is initiated upon entry of the POWER_UP state.

When the port output voltage has ramped-up, the port current will decrease and the HGATEn pin voltage will continue rising to fully enhance the external MOSFET. The final gate-to-source voltage for the MOSFET is ΔV_{HGATEn}. Power up is complete when the voltage between the IN pin and the port OUTPn pin drops below the high-side power good threshold voltage, ΔV_{OUTP_PWRGDn}.

If inrush is not complete within t_{INRUSH}, the port enters the RESTART state and the port’s t_{INRUSH} Timer Done bit is set (**p*n*ev.tinrush_timer_done**). The t_{INRUSH} timer limit is programmable (**p*n*cfg1.tinrush_timer**). If the inrush completes within t_{INRUSH}, the port proceeds to the POWER_ON state.

POWER_ON State

During operation in the POWER_ON state, the high-side output current is continuously monitored and limited by the port current sense ADC and an electronic circuit breaker with foldback Analog Current Limit (ACL), respectively. If the PD does not present a valid MFVS for more than t_{MFVDO}, the port goes to the SETTLE_SLEEP state and starts discharging the port output voltage to the range of V_{SLEEP}. If the host decides power is not available it can de-assert Port Software Power Available (**p*n*cfg0.sw_power_available**), and the port will go to the RESTART state.

SETTLE_SLEEP State

In the SETTLE_SLEEP state, the port output is discharged to V_{SLEEP} by pull-down current $I_{DISCHARGE}$. If the output voltage discharges to V_{SLEEP} within t_{OFF}, the port goes to the SLEEP state. A port will enter the OVERLOAD state from the SETTLE_SLEEP state if it is unable to discharge the port output to V_{SLEEP} within t_{OFF}.

SLEEP State

In the SLEEP state, the port output is maintained at V_{SLEEP} and monitored for a wakeup signature current, I_{WAKEUP}, from the PD. The PSE enters the DETECTION state after a valid wakeup signature is detected for at least t_{WAKEUP}. A wakeup event can also be initiated by the PSE application host microcontroller via SPI or the WAKEUP pin.

In the SLEEP state, an internal LDO will continue to bias the port output voltage to V_{SLEEP}. A PD in the PD_SLEEP state consumes less than I_{SLEEP_PD} (100µA). A PD may request the PSE re-apply full operating voltage by presenting the wakeup signature current, I_{WAKEUP_PD} (1.3mA to 1.8mA) for at least t_{WAKEUP_PD} (0.2ms minimum). If the PSE output current is in the range of I_{WAKEUP} for at least t_{WAKEUP}, the PSE is required to wake up and go to the DETECTION state. A PSE may or may not wake up in response to currents in the range of 0.5mA to 1.25mA and 1.85mA to 2.5mA. A PSE shall not wake up in response to currents less than 0.5mA or greater than 2.5mA. See Figure 47.

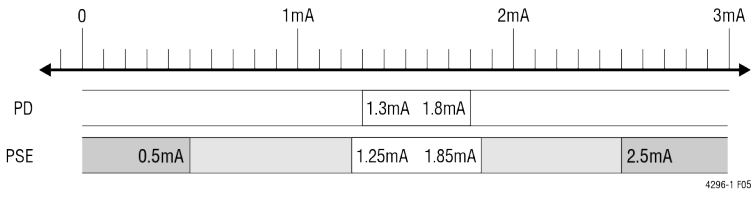


Figure 47. IEEE 802.3bu Wakeup Current Ranges

OPERATION

A port can disable PD initiated wakeup by setting the Upstream Wakeup Disable bit in the Port Configuration 0 register (***pn*cfg0.upstream_wakeup_disable**).

A port can also be forced to exit the SLEEP state by setting the Software Wakeup bit (***pn*cfg0.sw_pse_wakeup**). Alternatively, if Downstream Wakeup Disable bit (***pn*cfg0.downstream_wakeup_disable**) is not set, then the port can be forced to exit the SLEEP state by raising the WAKEUP pin.

RESTART State

In the RESTART state the port output is biased to V_{SLEEP}. A port will wait for at least $t_{RESTART}$ before re-entering the IDLE state. The $t_{RESTART}$ timer limits are programmable (***pn*cfg1.tod_trestart_timer**).

OVERLOAD State

A current overload fault can occur during any state except the DISABLED or DETECTION states. This fault will cause the port to enter the OVERLOAD state.

In the OVERLOAD state, the port high-side MOSFET is turned off and the port output voltage is discharges to $V_{DISABLE}$. The port waits t_{OD} before going to the IDLE state. The t_{OD} timer limits are programmable (***pn*cfg1.tod_trestart_timer**).

Maintain Full Voltage Signature (MFVS)

MFVS detection guarantees full operating voltage is applied only when a PD is connected and requires full power. A PD must draw more than 11mA to ensure it continues to receive full operating voltage. In the POWER_ON state, a port must consider MFVS present when the port current exceeds I_{HOLD}(max) (10mA) for at least t_{MFVS}. Port MFVS is absent when the port current drops below I_{HOLD}(min)(2.5mA) for at least t_{MFVDO}. A port may consider MFVS present or absent when the port current is in the range of I_{HOLD} (Figure 48). If MFVS is absent, the port enters the SETTLE_SLEEP state and discharge the port output voltage to the range of V_{SLEEP}.

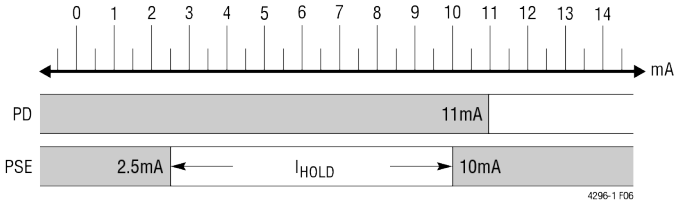


Figure 48. IEEE 802.3bu MFVS Current Ranges

The LTC4296-1 offers a number of advanced power management features. The WAKEUP pin can be used as a hardware interrupt to indicate a PD initiated wakeup or to forward a wakeup request, both of which can be disabled through SPI. The LTC4296-1 also has a very low current “Deep Sleep” mode, which is useful in battery powered applications, when all the ports are either in the DISABLED or SLEEP state.

A port can be forced to stay in the POWER_ON state if MFVS is absent by disabling the t_{MFVDO} timer (***pn*cfg0.tmfvdo_timer_disable**).

The MFVS threshold of a port is programmable (***pn*adccfg.mfvs_threshold**). Equation 1 gives the optimum code as a function of the high-side sense resistor, R1; the value is rounded to the nearest integer.

$$\text{MFVS Threshold Code} = 62.5 \cdot R1 \quad (1)$$

HOST SERIAL INTERFACE

The LTC4296-1 communicates with the system host using SPI. The $\overline{CS}$ input allows the host to select end device at a time for serial communication when multiple end devices share a common SPI bus.

SPI Clock Phase and Polarity

The LTC4296-1 operates in SPI Mode 3 (CPOL = 1, CPHA = 0, idle CLK = 1). Consequently, data on SDI must be stable during the rising edge of SCK as shown in Figure 49 and Figure 50 (Write and Read, respectively).

Data Transfers

Every command (read or write) is 1 byte long consisting of 7-bits of address and 1 read/write bit. Every register value is 2 bytes long. The command and data are transferred with the most significant bit (MSB) first.

On a write, the data value on SDI is latched into the device on the rising edge of SCK (Figure 49). Similarly, on a read, the data value output on SDO is valid during the rising edge of SCK and transitions on the falling edge of SCK (Figure 50). $\overline{CS}$ must remain low for the entire duration of a command sequence, including between a command byte and subsequent data.

PEC Byte

The packet error code (PEC) byte is a cyclic redundancy check (CRC) value calculated for all the bits in a register group in the order they are passed, using the initial PEC value of 0x41 and the following characteristic polynomial: x8 + x2 + x + 1

To calculate the 8-bit PEC value, a simple procedure can be established:

1. Initialize the PEC to 0x41.

2. For each data bit (DIN) coming into the register group, set IN0 = DIN XOR PEC[7], then IN1 = PEC[0] XOR IN0, IN2 = PEC[1] XOR IN0.

3. Update the 8-bit PEC as PEC[7] = PEC[6], PEC[6] = PEC[5]..... PEC[3] = PEC[2], PEC[2] = IN2, PEC[1] = IN1, PEC[0] = IN0.

4. Go back to Step 2 until all data are shifted. The 8-bit result is the final PEC byte.

OPERATION

For a given SPI transaction, the PEC byte is calculated over the entire command byte which includes the address and a read/write bit, using the above procedure. The PEC byte is then re-initialized to 0x41 for subsequent data word reads or writes. The PEC byte is calculated for each data word separately.

LTC4296-1 calculates a PEC byte for any command or data received and compares it with the PEC byte received following the command or data. The command or data is regarded as valid only if the PEC bytes match. For a SPI read operation, LTC4296-1 attaches the calculated PEC byte at the end of the data it shifts out on the SDO pin.

Serial data transactions with an invalid command byte sequence or PEC byte result in the Command Fault bit (**gfltev.command_fault**) or PEC Fault bit (**gfltev.pec_fault**), respectively, being set in the Global Fault Event register. The Global Command register can also be used to protect the registers from unintended writes by writing a code to disable the write access to the register map. To enable write access after a reset event, the host must first unlock the LTC4296-1 by writing the unlock key in the Global Command register (**gcmd.write_protect**). See Register Descriptions.

Figure 51 provides a pseudo code implementation of SPI write and read operations with PEC.

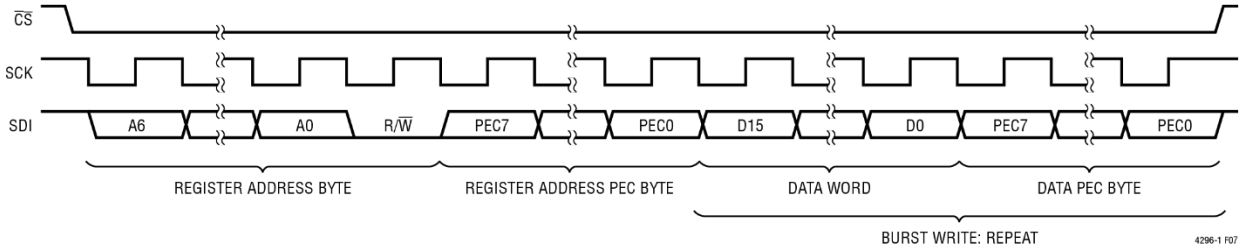


Figure 49. SPI Write

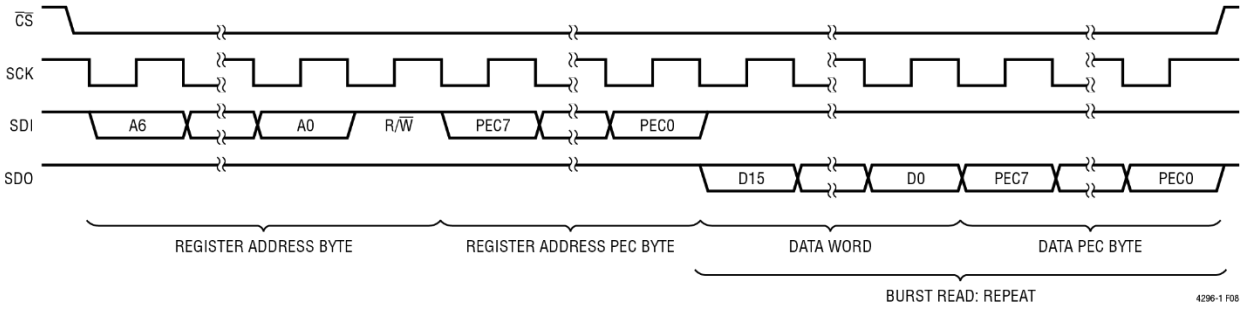


Figure 50. SPI Read

SAMPLE CODE

```
//*************************************************************************
// Copyright 2022 Analog Devices, Inc.
// All rights reserved.
//
// EXAMPLE: LTC4296-1 SPI PEC Calculation and Read/Write Transactions in C
//*************************************************************************/

uint8_t get_pec_byte(uint8_t data, uint8_t seed)
{
    uint8_t pec = seed;
    uint8_t din, in0, in1, in2;
    int bit;
    for(bit=7; bit>=0; bit--)
    {
        din = (data>>bit) & 0x01;
        in0 = din ^ ( (pec>>7) & 0x01 );
        in1 = in0 ^ ( pec & 0x01);
        in2 = in0 ^ ( (pec>>1) & 0x01 );
        pec = (pec << 1);
        pec &= ~(0x07);
        pec = pec | in0 | (in1<<1) | (in2<<2);
    }
    return pec;
}

void example_write(uint8_t register_address, uint16_t value)
{
    uint8_t tx_buf[5];
    // command byte: register address with r/w bit
    tx_buf[0] = (register_address << 1) & ~(0x01); // r/w bit = 0 for write

    // pec byte from command byte
    tx_buf[1] = get_pec_byte(tx_buf[0], 0x41);

    // data word: 2 bytes, MSB first
    tx_buf[2] = value >> 8;   // MSB
    tx_buf[3] = value & 0xFF; // LSB

    // pec byte from data word by using pec calculation twice
    uint8_t intermediate = get_pec_byte(tx_buf[2], 0x41);
    tx_buf[4] = get_pec_byte(tx_buf[3], intermediate);

    // transmit 5 bytes on spi bus
    spi_tx(tx_buf, 5);
}
uint16_t example_read(uint8_t register_address)
{
    uint8_t tx_buf[2];
    uint8_t rx_buf[3];

    // command byte: register address with r/w bit
    tx_buf[0] = (register_address << 1) | 0x01;

    // pec byte from command byte
    tx_buf[1] = get_pec_byte(tx_buf[0], 0x41);

    // transmit command byte and pec byte
    spi_tx(tx_buf,2);

    // receive data word and pec byte into rx_buf
    spi_rx(rx_buf,3);

    // construct register value from received data word
    uint16_t register_value = ((uint16_t)rx_buf[0] << 8) |
(uint16_t)rx_buf[1];

    return register_value;
}
//*************************************************************************/
```

Figure 51. Pseudo Code Implementation of SPI Write and Read Operations with PEC

Table 5. Register Summary

ADDRESS†	REGISTER NAME	R/W	PORT	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	RESET STATE
Global Events																				
0x02	gfltev	W1C	g	reserved											uvlo_digital	command_fault	pec_fault	memory_fault	low_ckt_brk_fault	0x0010
0x03	gfltmsk	R/W	g	reserved												command_fault	pec_fault	memory_fault	low_ckt_brk_fault	0x000F
Global Status																				
0x06	gcap	RO	g	reserved									sccp_support	wake_fwd_support	numports					0x0025
0x07	giost	RO	g	reserved							pg_out4	pg_out3	pg_out2	pg_out1	pg_out0	pad_auto	pad_wakeup	pad_wakeup_drive	reserved	0x0000
Command																				
0x08	gcmd	R/W	g	sw_reset							write_protect									0x00A0
Configuration																				
0x09	gcfg	R/W	g	reserved										mask_lowfault	tlim_disable	tlim_timer_sleep		refresh	sw_vin_pgood	0x0009
Global ADC																				
0x0A	gadccfg	R/W	g	reserved									gadc_sample_mode	gadc_sel						0x0000
0x0B	gadcdat	RO	g	reserved		gadc_missed	gadc_new	gadc												0x0000
Port0 Events																				
0x10	p0ev	W1C	0	reserved						valid_signature	invalid_signature	toff_timer_done	overload_detected_isleep	overload_detected_ipowered	mfvs_timeout	tinrush_timer_done	pd_wakeup	lsns_forward_fault	lsns_reverse_fault	0x0000
Port0 Status																				
0x12	p0st	RO	0	reserved		det_vhigh	det_vlow	power_stable_hi	power_stable_lo	power_stable	overload_held	pi_sleeping	pi_prebiased	pi_detecting	pi_powered	pi_discharge_en	pse_status			0x0000
Port0 Configuration																				
0x13	p0cfg0	R/W	0	sw_inrush	end_classification	set_classification_mode	disable_detection_pullup	tdet_disable	foldback_disable	soft_start_disable	toff_timer_disable	tmfvdo_timer_disable	sw_pse_ready	sw_power_available	upstream_wakeup_disable	downstream_wakeup_disable	sw_pse_wakeup	hw_en_mask	sw_en	0x0002

Table 5. Register Summary

0x14	p0cfg1	R/W	0	reserved							prebias_override_good	tlim_timer_top		tod_trestart_timer		tinrush_timer	sig_override_bad	sig_override_good	0x0008
0x15	p0adccfg	R/W	0	reserved								mfvs_threshold							0x0006
0x16	p0adcdat	RO	0	reserved			missed	new	source_current										0x0000
Port0 Diagnosis																			
0x17	p0selftest	R/W	0	reserved													force_bad_outm	force_bad_outp	0x0000
Port1 Events																			
0x20	p1ev	W1C	0	reserved						valid_signature	invalid_signature	toff_timer_done	overload_detected_isleep	overload_detected_ipowered	mfvs_timeout	tinrush_timer_done	pd_wakeup	lsns_forward_fault	lsns_reverse_fault	0x0000
Port1 Status																			
0x22	p1st	RO	1	reserved			det_vhigh	det_vlow	power_stable_hi	power_stable_lo	power_stable	overload_held	pi_sleeping	pi_prebiased	pi_detecting	pi_powered	pi_discharge_en	pse_status		0x0000
Port1 Configuration																			
0x23	p1cfg0	R/W	0	sw_inrush	end_classification	set_classification_mode	disable_detection_pullup	tdet_disable	foldback_disable	soft_start_disable	toff_timer_disable	tmfvdo_timer_disable	sw_pse_ready	sw_power_available	upstream_wakeup_disable	downstream_waekup_disable	sw_pse_wakeup	hw_en_mask	sw_en	0x0002
0x24	p1cfg1	R/W	0	reserved							prebias_override_good	tlim_timer_top		tod_trestart_timer		tinrush_timer		sig_override_bad	sig_override_good	0x0008
0x25	p1adccfg	R/W	1	reserved								mfvs_threshold								0x0006
0x26	p1adcdat	RO	1	reserved			missed	new	source_current											0x0000
Port1 Diagnosis																			
0x27	p1selftest	R/W	1	reserved														force_bad_outm	force_bad_outp	0x0000
Port2 Events																			
0x30	p2ev	W1C	0	reserved						valid_signature	invalid_signature	toff_timer_done	overload_detected_isleep	overload_detected_ipowered	mfvs_timeout	tinrush_timer_done	pd_wakeup	lsns_forward_fault	lsns_reverse_fault	0x0000
Port2 Status																			

Table 5. Register Summary

0x32	p2st	RO	2	reserved		det_vhigh	det_vlow	power_stable_hi	power_stable_lo	power_stable	overload_held	pi_sleeping	pi_prebiased	pi_detecting	pi_powered	pi_discharge_en	pse_status		0x0000
Port2 Configuration																			
0x33	p2cfg0	R/W	2	reserved				tdet_disable	foldback_disable	soft_start_disable	toff_timer_disable	tmfvdo_timer_disable	sw_pse_ready	sw_power_available	upstream_wakeup_disable	downstream_wakeup_disable	sw_pse_wakeup	hw_en_mask	sw_en	0x0002
0x34	p2cfg1	R/W	2	reserved								tlim_timer_top		tod_trestart_timer		tinrush_timer		sig_override_bad	sig_override_good	0x0000
0x35	p2adccfg	R/W	2	reserved								mfvs_threshold								0x0006
0x36	p2adcdat	RO	2	reserved		missed	new	source_current												0x0000
Port2 Diagnosis																			
0x37	p2selftest	R/W	2	reserved														force_bad_outm	force_bad_outp	0x0000
Port3 Events																			
0x40	p3ev	W1C	0	reserved						valid_signature	invalid_signature	toff_timer_done	overload_detected_isleep	overload_detected_ipowered	mfvs_timeout	tinrush_timer_done	pd_wakeup	lsns_forward_fault	lsns_reverse_fault	0x0000
Port3 Status																			
0x42	p3st	RO	3	reserved		det_vhigh	det_vlow	power_stable_hi	power_stable_lo	power_stable	overload_held	pi_sleeping	pi_prebiased	pi_detecting	pi_powered	pi_discharge_en	pse_status			0x0000
Port3 Configuration																			
0x43	p3cfg0	R/W	0	sw_inrush	end_classification	set_classification_mode	disable_detection_pullup	tdet_disable	foldback_disable	soft_start_disable	toff_timer_disable	tmfvdo_timer_disable	sw_pse_ready	sw_power_available	upstream_wakeup_disable	downstream_wakeup_disable	sw_pse_wakeup	hw_en_mask	sw_en	0x0002
0x44	p3cfg1	R/W	0	reserved							prebias_override_good	tlim_timer_top		tod_trestart_timer		tinrush_timer		sig_override_bad	sig_override_good	0x0008
0x45	p3adccfg	R/W	3	reserved								mfvs_threshold								0x0006
0x46	p3adcdat	RO	3	reserved		missed	new	source_current												0x0000
Port3 Diagnosis																			
0x47	p3selftest	RW	3	reserved														force_bad_outm	force_bad_outp	0x0000

Table 5. Register Summary

Port4 Events																			
0x50	p4ev	W1C	0	reserved						valid_signature	invalid_signature	toff_timer_done	overload_detected_isleep	overload_detected_ipowered	mfvs_timeout	tinrush_timer_done	pd_wakeup	lsns_forward_fault	lsns_reverse_fault	0x0000
Port4 Status																			
0x52	p4st	RO	4	reserved		det_vhigh	det_vlow	power_stable_hi	power_stable_lo	power_stable	overload_held	pi_sleeping	pi_prebiased	pi_detecting	pi_powered	pi_discharge_en	pse_status			0x0000
Port4 Configuration																			
0x53	p4cfg0	R/W	0	sw_inrush	end_classification	set_classification_mode	disable_detection_pullup	tdet_disable	foldback_disable	soft_start_disable	toff_timer_disable	tmfvdo_timer_disable	sw_pse_ready	sw_power_available	upstream_wakeup_disable	downstream_wakeup_disable	sw_pse_wakeup	hw_en_mask	sw_en	0x0002
0x54	p4cfg1	R/W	0	reserved							prebias_override_good	tlim_timer_top		tod_trestart_timer		tinrush_timer		sig_override_bad	sig_override_good	0x0008
0x55	p4adccfg	R/W	4	reserved								mfvs_threshold								0x0006
0x56	p4adcdat	RO	4	reserved		missed	new	source_current												0x0000
Port4 Diagnosis																			
0x57	p4selftest	R/W	4	reserved														force_bad_outm	force_bad_outp	0x0000

FIELD ACCESS KEY:

RO = Read Only. No effect of write operation. No effect of read operation. Reads back current value.

W1C = Write 1 to Clear. If the bit in the written value is 1, then that bit will be set to 0, else it will not be affected. No effect of read operation. Reads back current value.

R/W = Read/Write. Write changes the value to the written value. Read has no effect. Reads back current value.

WO = Write Only. Write changes the value to the written value. Read has no effect. Read back value undefined/dont_care.

† Addresses not listed in the table are reserved and should not be written to.

REGISTER MAP

GLOBAL EVENTS

Table 6. gfltev (Address 0x02): Global Fault Event Register, Write 1 to Clear. Indicates Presence of Global Level Faults.

BIT(S)	NAME	DESCRIPTION
15:5	reserved	For future use
4	uvlo_digital	Set if digital core has been in UVLO. This is an unmaskable interrupt
3	command_fault	Set if an invalid or disallowed command has been sent by host. (e.g. accessing invalid register address)
2	pec_fault	Set if a PEC fault has occurred during SPI transaction
1	memory_fault	Set if fault(s) has/have occurred in memory
0	low_ckt_brk_fault	Set if one or more circuit breakers has/have been tripped in the return path or if there is a fault in the deep sleep return path

Table 7. gfltmsk (Address 0x03): Global Fault Event Mask Register, Read/Write. Provides Mask for the Global Level Fault Events.

BIT(S)	NAME	DESCRIPTION
15:4	reserved	For future use
3	command_fault	If this bit is cleared command interrupt is cleared
2	pec_fault	If this bit is cleared PEC interrupt is cleared
1	memory_fault	If this bit is cleared memory interrupt is cleared
0	low_ckt_brk_fault	If this bit is cleared return path interrupt is cleared

GLOBAL STATUS

Table 8. gcap (Address 0x06): Global Capability Register, Read Only. Presents Supported Features of PoDL Standard.

BIT(S)	NAME	DESCRIPTION
15:7	reserved	For future use
6	sccp_support	Set to 1 if Serial Communications Classification Protocol is supported (SCCP is not supported by the LTC4296-1 without external micro-controller support)
5	wake_fwd_support	Set to 1 if wakeup forwarding is supported (wakeup forwarding is supported by the LTC4296-1)
4:0	numports	Number of PSE ports

Table 9. giost (Address 0x07): Global Status Register, Read Only. Presents Status of the IOs.

BIT(S)	NAME	DESCRIPTION
15:9	reserved	For future use
8	pg_out4	Status of port4 power good
7	pg_out3	Status of port3 power good
6	pg_out2	Status of port2 power good
5	pg_out1	Status of port1 power good
4	pg_out0	Status of port0 power good
3	pad_auto	Status of AUTO pin
2	pad_wakeup	Status of WAKEUP pin as driven by the host
1	pad_wakeup_drive	Status of WAKEUP pin as driven by the IC
0	reserved	For future use

COMMAND

Table 10. gcmd (Address 0x08): Global Command Register, Read/Write. Entry Point for the Host to Configure the Chip.

BIT(s)	NAME	DESCRIPTION
15:8	sw_reset	After writing reset code (0x73) in this field, the digital logic is reset (software reset)
7:0	write_protect	After writing write unlock key (0x05), write access to all writeable registers is enabled. After writing write lock key (0xA0), write access to all writeable registers is disabled. Write access to this field is always enabled

REGISTER MAP

CONFIGURATION

Table 11. gcfg (Address 0x09): Global Configuration Register, Read/Write. Enable the Host to Configure Global Functions.

BIT(S)	NAME	DESCRIPTION
15:6	reserved	For future use
5	mask_lowfault	Write 1 to prevent ports from entering overload due to low-side faults
4	tlim_disable	Write 1 to disable t_{lim} timers of all ports
3:2	tlim_timer_sleep	Configures the sleep regulator fault timer for all the ports and the deep sleep return path fault timer as shown below: 00b – 15.6ms 01b – 31.2ms 10b – 62.5ms (default) 11b – disable sleep fault timers
1	refresh	Write 1 to copy contents from non-volatile memory into volatile memory. Auto cleared after completion.
0	sw_vin_pgood	Write 1 to indicate that the system is ready to source the required power to connected PD(s).

GLOBAL ADC

Table 12. gadccfg (Address 0x0A): Global ADC Configuration Register, Read/Write. Allows the Host to Configure the Global ADC.

BIT(S)	NAME	DESCRIPTION
15:7	reserved	For future use
6:5	gadc_sample_mode	Configures global ADC in following modes as follows: 00b – disabled 01b – single-shot mode (auto cleared after one measurement) 10b – continuous mode with low gain 11b – continuous mode with high gain
4:0	gadc_sel	Configures global ADC inputs as follows: 00000b – GND 00001b – V_{IN} 00010b – Temperature 00100b – Port 0 output voltage 00101b – Port 0 return sense voltage 00110b – Port 1 output voltage 00111b – Port 1 return sense voltage 01000b – Port 2 output voltage 01001b – Port 2 return sense voltage 01010b – Port 3 output voltage 01011b – Port 3 return sense voltage 01100b – Port 4 output voltage 01101b – Port 4 return sense voltage 1XXXXb – Internal check voltage reference

Table 13. gadcdat (Address 0x0B): Global ADC Data Rregister, Read Only. Allows the Host to Read the Latest Global ADC Measurement.

BIT(S)	NAME	DESCRIPTION
15:14	reserved	For future use
13	gadc_missed	Set when host has missed reading one or more result(s) stored by the global ADC in **gadcdat.gadc**
12	gadc_new	Set when a new result is stored by the global ADC in **gadcdat.gadc**
11:0	gadc	Global ADC accumulation result

REGISTER MAP

PORTN EVENTS

Table 14. pnev (Address 0xm0): Portn Event Register, Write 1 to Clear. Indicates presence of Portn Events.

BIT(S)	NAME	DESCRIPTION
15:10	reserved	For future use
9	valid_signature	Set when a valid signature was detected on the port
8	invalid_signature	Set when an invalid signature was detected on the port
7	toff_timer_done	Set when t_{OFF} timer expired when port was discharging toward V_{SLEEP}
6	overload_detected_isleep	Set when overload timer t_{LIM} expired due to overcurrent while the port was attempting to apply V_{SLEEP} at the PI
5	overload_detected_ipowered	Set when overload timer t_{LIM} expired due to overcurrent while the port was in the POWER_UP or POWER_ON state
4	mfvs_timeout	Set when power was removed due to t_{MFVDO} timer expiration
3	tinrush_timer_done	Set when t_{INRUSH} timer expired when the port was in the POWER_UP state
2	pd_wakeup	Set when an upstream (PD initiated) wakeup was detected i.e. the port current was in the valid wakeup current range for at least t_{WAKEUP} when the port was in the SLEEP state
1	lsns_forward_fault	Set when low-side forward circuit breaker fault event has occurred on the port
0	lsns_reverse_fault	Set when low-side reverse circuit breaker fault event has occurred on the port

REGISTER MAP

PORTN STATUS

Table 15. pnst (Address 0xm2): Portn Status Register, Read Only. Provides Status of Portn Events.

BIT(S)	NAME	DESCRIPTION
15:14	reserved	For future use
13	det_vhigh	Set when port voltage is greater than $V_{BAD\_HI\_PSE}$ during DETECTION
12	det_vlow	Set when port voltage is less than $V_{BAD\_LO\_PSE}$ during DETECTION
11	power_stable_hi	Set when following inrush port is sourcing full operating voltage and V_{IN} - V_{OUTPn} is less than ΔV_{OUTP_PWRGDn}
10	power_stable_lo	Set when following inrush port is sourcing full operating voltage and V_{OUTMn} less than delta ΔV_{OUTM_PWRGDn}
9	power_stable	Set when the port is delivering full operating voltage to the output.
8	overload_held	Set when the port is in the OVERLOAD state
7	pi_sleeping	Set when the port is in the SETTLE_SLEEP or SLEEP state
6	pi_prebiased	Set when the port is in the IDLE state
5	pi_detecting	Set when the port is in the DETECTION state
4	pi_powered	Set when the port is in the POWER_UP or POWER_ON state
3	pi_discharge_en	Set when the port is in the SETTLE_SLEEP state
2:0	pse_status	PSE status decoded as below: 000b – Port is disabled 001b – Port is in sleeping 010b – Port is delivering power 011b – Port is searching 100b – Port is in error 101b – Port is idle 110b – Port is preparing for detection 111b – Port is in an unknown state

PORTN CONFIGURATION

Table 16. pncfg0 (Address 0xm3): Portn Configuration Register 0, Read/Write, 0x0002; Provides Portn Configuration.

BIT(S)	NAME	DESCRIPTION
15	sw_inrush	Write 1 to skip prebias and detection and directly power up the PD
14	end_classification	Write 1 to end classification. Auto cleared by the IC.
13	set_classification_mode	Write 1 to set the port in Classification mode
12	disable_detection_pullup	Write 1 to disable detection pullup current
11	tdet_disable	Write 1 to disable detection timer
10	foldback_disable	Write 1 to disable foldback during port inrush in the POWER_UP state
9	soft_start_disable	Write 1 to disable soft start during port inrush in the POWER_UP state
8	toff_timer_disable	Write 1 to disable the t_{OFF} timer to allow the port arbitrarily long time for discharging in the SETTLE_SLEEP state
7	tmfvdo_timer_disable	Write 1 to disable the t_{MFVDO} timer to prevent the port from shutting off in absence of a valid MFVS
6	sw_pse_ready	Write 1 to indicate that the port is ready for detection
5	sw_power_available	Write 1 to indicate that the port is able to source power to the connected PD
4	upstream_wakeup_disable	Write 1 to disable the upstream (PD initiated) wakeup of the port
3	downstream_wakeup_disable	Write 1 to disable the downstream (PSE initiated) wakeup of the port
2	sw_pse_wakeup	Write 1 to wake up the port
1	hw_en_mask	Write 0 to mask the AUTO pin
0	sw_en	Write 1 to enable the port

REGISTER MAP

Table 17. pncfg1 (Address 0xm4): Portn Configuration Register 1, Read/Write. Provides Portn Configuration.

BIT(S)	NAME	DESCRIPTION
15:9	reserved	For future use
8	prebias_override_good	Write 1 to simulate a valid wakeup signature
7:6	tlim_timer_top	Write as below to configure the topside fault timer (t_{LIM}): 00b – 59.9ms (default) 01b – 29.9ms 10b – 15ms 11b – 0.46ms Note: t_{LIM} timer will decrement towards zero in presence of fault event and increment towards the configured value in absence of fault event. The decrement rate will be 8x the increment rate
5:4	tod_trestart_timer	Write as below to configure the overload delay timer and restart timer: 00b – default (t_{OD} = 1.1s, $t_{RESTART}$ = 551ms) 01b – 2x of default 10b – 4x of default 11b – forever
3:2	tinrush_timer	Write as below to configure the t_{inrush} timer: 00b – 3.5ms 01b – 14ms 10b – 56.2ms(default) 11b – forever
1	sig_override_bad	Write 1 to simulate an invalid detection voltage signature
0	sig_override_good	Write 1 to simulate a valid detection voltage signature

Table 18. pnadccfg (Address 0xm5): Portn ADC Configuration Register, Read/Write. Provides Portn ADC configuration.

BIT(S)	NAME	DESCRIPTION
15:8	reserved	For future use
7:0	mfvs_threshold	MFVS threshold to be set based on Equation 1

Table 19. pnadcdat (Address 0xm6): Portn ADC Data Register, Read Only. Allows the Host to Read the Latest Portn ADC measurement.

BIT(S)	NAME	DESCRIPTION
15:14	reserved	For future use
13	missed	Set when host has missed one or more measurements of source current stored in **pnadcdat.source_current**
12	new	Set when a new measurement result of source current is stored by the port ADC in **pnadcdat.source_current**
11:0	source_current	Source current measurement

PORTN DIAGNOSIS

Table 20. pnselftest (Address 0xm7): Portn Self Test Register, Read/Write. Enable the Host to Perform Diagnosis on Portn.

BIT(S)	NAME	DESCRIPTION
15:2	reserved	For future use
1	force_bad_outm	Write 1 to simulate a power bad on OUTM pin of the port
0	force_bad_outp	Write 1 to simulate a power bad on OUTP pin of the port

APPLICATIONS INFORMATION

APPLICATION OVERVIEW

Figure 52 shows a typical LTC4296-1 circuit for one of five ports. Each port high-side electronic circuit breaker with foldback analog current limit (ACL) controls inrush current during power up and protects against output faults. The circuit breaker controls N-channel MOSFET M1's gate-to-source voltage with the HGATEn and OUTPn pins while monitoring current sense resistor R1's voltage with the HSNSPn and HSNSMn pins. The port power snubber (R3 + R4, C4) stabilizes the ACL; it is disconnected by MOSFET M2 during classification. The auxiliary snubber (R5, C5) provides a well-defined AC impedance when switch M2 is disabled. The MOSFET M3 is driven by the host microcontroller to assert a logic low during SCCP write operation. The NPN transistor Q1 limits the voltage sensed by the microcontroller during SCCP.

Power controlled by the LTC4296-1 and data from a PHY, such as the ADIN1100, are coupled to the port through a power coupling network circuit. A common mode choke (CMC) and diplexer inductors comprise the power coupling network as further discussed in the Power Coupling Networks section.

POWER SUPPLY

When selecting a power supply, the tolerance of the supply and the voltage drops across the power path components at the highest PD load must fall within the V_{PSE} range specified in Table 1 for the desired Class. The LTC4296-1 is designed to service up to five ports that share the same voltage class (24V or 54V).

In order to ensure data integrity, the PSE power supply at the LTC4296-1 input needs to meet ripple specifications as required by IEEE 802.3cg. Ripple should be measured at the medium dependent interface (MDI) connector with a DSO using the AC coupled 100Ω resistor and scope probe shown in Figure 53. The observed ripple should be less than $0.1V_{PP}$ in a bandwidth of 1kHz to 10MHz. The observed ripple is then post processed with a transfer function $H(f)$ given by Equation 2 and should be less than $0.01V_{PP}$ in a bandwidth of 1kHz to 10MHz.

$$H(f) = \frac{f}{\sqrt{f^2 + f_0^2}} \text{ where } f_0 = 100\text{kHz} \quad (2)$$

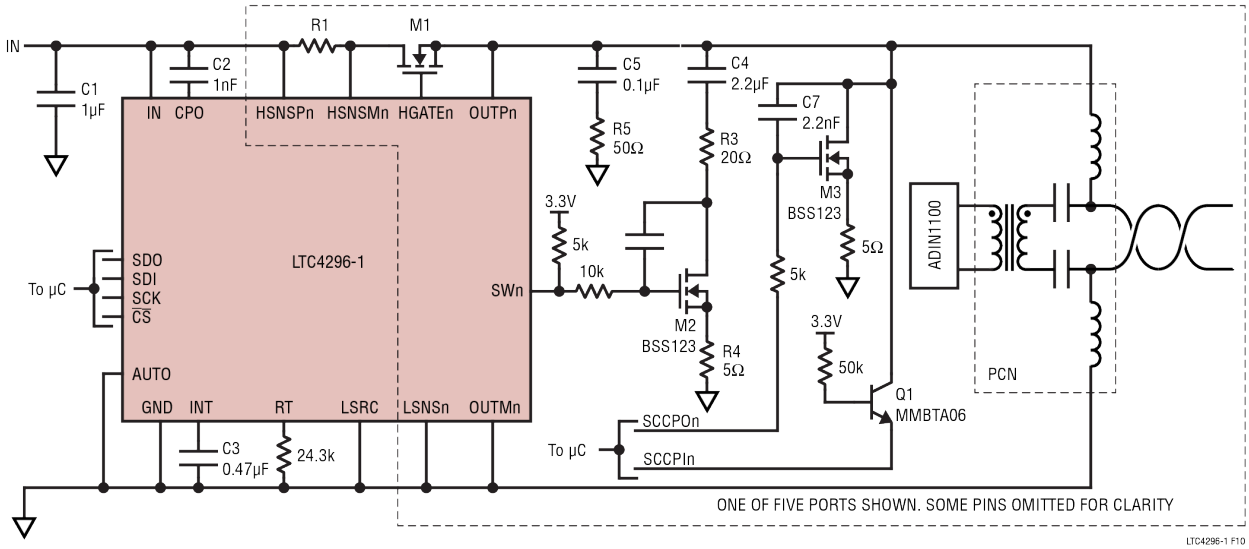


Figure 52. Typical LTC4296-1 Circuit (1 of 5 ports Shown)

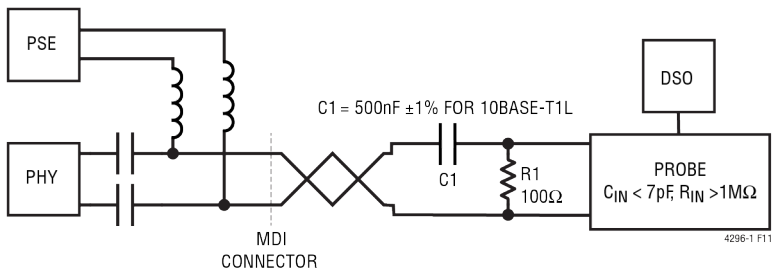


Figure 53. Power Supply Ripple Measurement Setup

APPLICATIONS INFORMATION

EXTERNAL COMPONENT SELECTION

Typical application components for Class 10-14 are shown in the Figure 54 schematic and table. Typical application components for Class 15 are shown in Figure 55 schematic. Additional guidance on selecting components is provided here.

Capacitors

The LTC4296-1 IN pin operates from an input voltage between 6V and 60V. A low ESR decoupling capacitance (C1) of at least 1µF should be placed from IN to GND. Common ceramic capacitors have significant voltage coefficients; the capacitance is reduced as the applied voltage increases. To minimize this problem, the IN pin bypass capacitor should be rated X7R and twice the maximum operating voltage.

The LTC4296-1 generates its own internal supplies at the INT and CPO pins. A 470nF, 6.3V decoupling capacitor (C3) should be placed from INT to GND and a 1nF, 16V decoupling capacitor (C2) should be placed from CPO to IN. Capacitors C1, C4, C5, C6, C7, C8, and C9 must have proper supply voltage ratings for the Class Applications.

Input TVS

A TVS across the supply helps protect the LTC4296-1 (and any other device on this rail) from overvoltage due to supply spike during a cable surge or forced backfeed voltages. The TVS clamp voltage and power rating should meet the surge current requirements and maximum voltage ratings of devices on the rail.

High-Side MOSFET

The LTC4296-1 provides a foldback ACL feature which reduces the port current limit threshold voltage when the MOSFETs drain to source voltage exceeds 12V. Foldback may be disabled via software. A port high-side N-channel MOSFET (M1) with adequate safe operating area (SOA) consistent with the foldback analog current limit profile must be used to ensure reliability during inrush and short-circuit conditions. Refer to the Analog Foldback Current Limit Threshold Voltage vs. V_{IN} - V_{OUTPn} typical curve. This curve is scaled for current with the port's sense resistor value for comparison against a MOSFET SOA curve. The MOSFET SOA curve must meet this foldback curve for t_{INRUSH} and t_{LIM}, and the system's maximum operating ambient temperature.

Additional considerations when selecting a MOSFET are $R_{DS(ON)}$ and V_{DS}. Low $R_{DS(ON)}$ will minimize heat losses for port DC currents. The drain-source voltage must be specified above the power supply peak voltage.

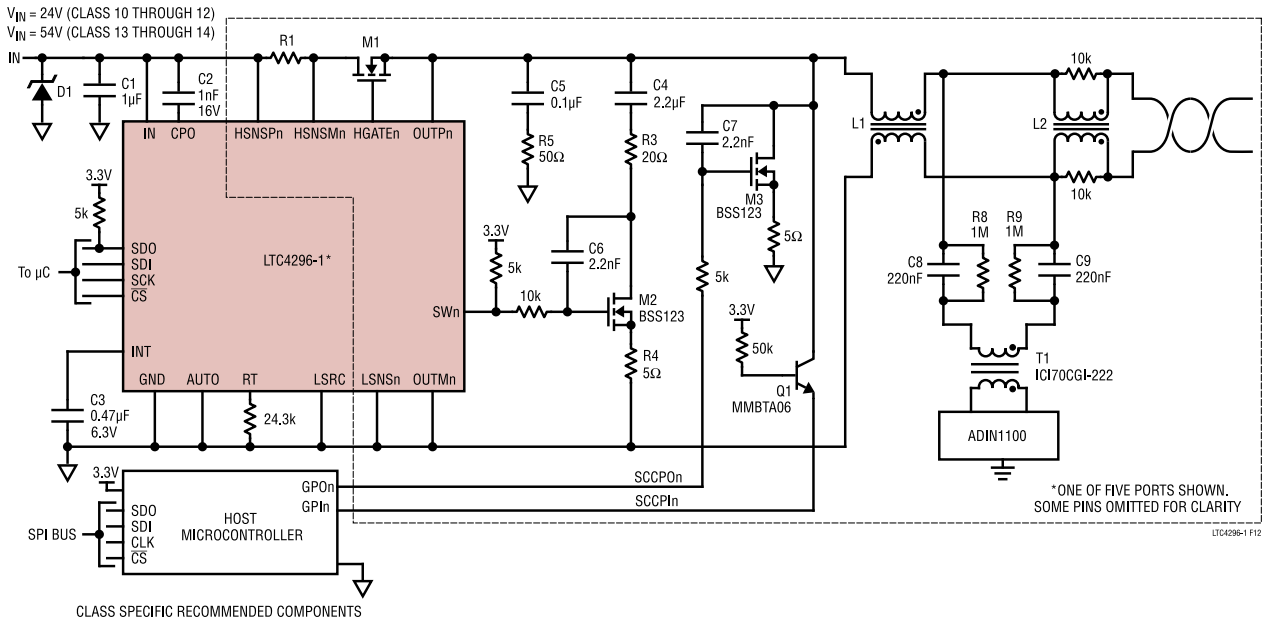
Figure 54 and Figure 55 provide a high-side N-channel MOSFET recommendation that meets the SOA requirements for each respective Class.

High-Side Sense Resistor

The LTC4296-1 is designed to work with a range of sense resistors required to meet IEEE 802.3cg's power Class requirements. A sense resistor for each port sets the respective port's high side ACL current threshold (I_{LIM}) per Equation 3. The ACL threshold must be in the range $I_{PI(MAX)} < I_{LIM} < 1.41 \bullet I_{PI(MAX)}$.

$$R1 < \Delta V_{HSNS\_ILIM(MIN)}/I_{LIM}\ (\Omega) \quad (3)$$

APPLICATIONS INFORMATION



CLASS SPECIFIC RECOMMENDED COMPONENTS

IEEE 802.3cg PSE CLASS	INPUT TVS (D1)	CAPACITOR VOLTAGE, TEMPERATURE RATING, (C1, C4, C5, C6, C7, C8, C9)	HIGH-SIDE SENSE RESISTOR (R1)	HIGH-SIDE MOSFET (M1)	SPoE INDUCTOR (L1)	POWER + DATA CMC (L2)
CLASS 10	SMAJ33A, 33V	50V, X7R	1.6Ω, 1/10W	BUK7M45-40E BUK7M21-40E	MSD7342-683 PID75-650M	DR334A-474BE RCM70CGI-471
CLASS 11			0.62Ω, 1/10W			
CLASS 12			0.24Ω, 1/4W	BUK7M12-40E	MSD1048H-683 PID100-650M	SRF0905A-471Y RCM70CGI-471
CLASS 13	SMAJ58A, 58V	100V, X7R	0.68Ω, 1/10W	PSMN075-100MSE	MSD7342-683 PID75-650M	DR334A-474BE RCM70CGI-471
CLASS 14			0.27Ω, 1/4W		MSD1048H-683 PID100-650M	SRF0905A-471Y RCM70CGI-471

Figure 54. LTC4296-1 802.3cg Class 10 through 14 Application

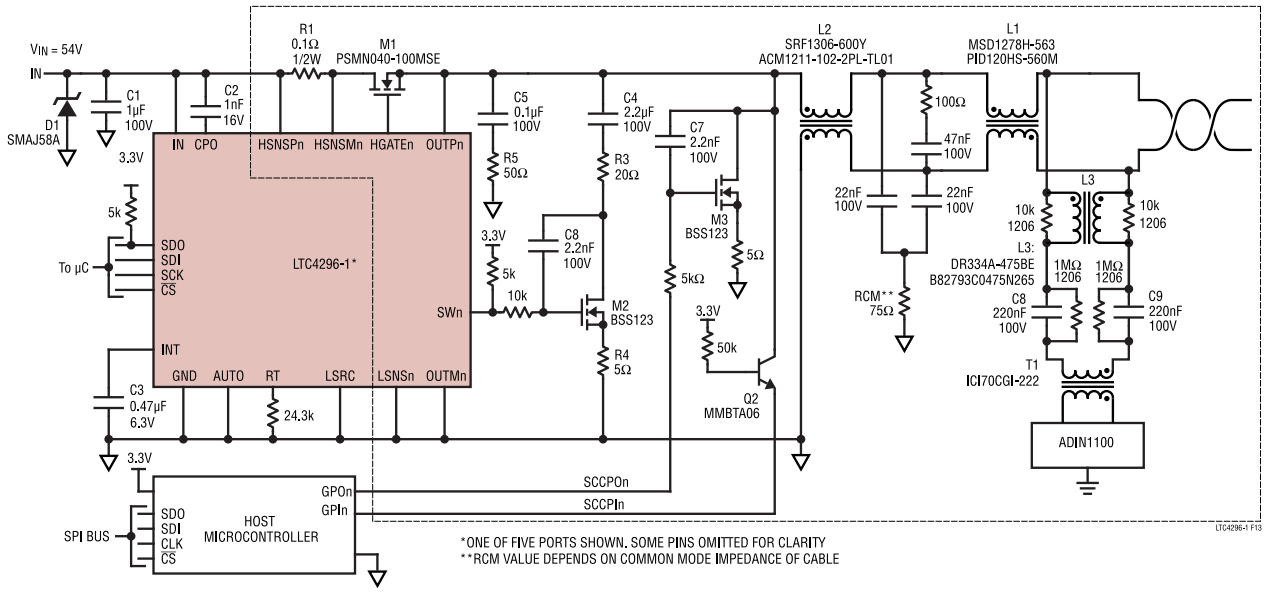


Figure 55. LTC4296-1 802.3cg Class 15 Application

APPLICATIONS INFORMATION

The sense resistors should have ±1% tolerance or better and no more than a ±200ppm/°C temperature coefficient. Appropriate wattage should be selected for the sense resistors per Equation 4. It is good practice to select a power rating for at least double the resistor application power.

$$P_{R1} > 2 \bullet (\Delta V_{HSNS\_ILIM9(MAX)})^2/R_1 \text{ (W)} \quad (4)$$

Figure 54 and Figure 55 provide a high-side sense resistor value and power rating for each 802.3cg power class.

Refer to the Layout Guidelines section for proper Kelvin Sensing with the sense resistor.

Power Coupling Networks

Power and data are coupled together at the MDI through a Power Coupling Network (PCN). The PHY is AC coupled through a data transformer (T1). The PSE DC power is coupled on to the differential data lines through the Differential Mode Inductor (DMI), L1. The Common Mode Choke (CMC), L2, blocks common mode signals at the MDI.

The DMI (L1) and CMC (L2) must be selected to meet the droop, return loss and mode conversion specifications as defined in the IEEE 802.3cg for the respective maximum power Class.

Figure 54 shows a PHY-side PCN topology; power is injected through the DMI (L1) on the PHY-side of the CMC (L2). Power and data is passed through the CMC. DC blocking capacitors (C8, C9) with balancing resistors (R8, R9) prevent the SPoE DC current from passing through transformer T1. This topology is recommended for Class 10 through 14.

Figure 55 shows a line-side (cable side) PCN topology for Class 15; power is injected through the DMI (L1) on the line-side of the PHY CMC (L3). L2 is the power path CMC and L3 is the data-only CMC. Capacitor, C8, blocks SPoE DC current from flowing through transformer T1.

Output Power Snubber

An output power snubber, comprised of a 2.2µF, X7R capacitor (C4) in series with a resistance (R3 + R4), from each port's OUTP to OUTM pins is required for current limit stability during startup or overload. The voltage rating of C4 must be at least twice the maximum operating voltage to account for capacitor voltage coefficients. For calculating R3 resistance, use Equation 5. Choose the nearest 5% resistor values.

$$R3 = 2 \bullet \sqrt{\frac{L_{DIFF}}{C4}} - R4 \quad (5)$$

L_{DIFF} is the differential inductance between OUTPn and OUTMn at L1. If L1 is a DMI (coupled inductor) use the calculated differential inductance of four times the single winding inductance. The 5Ω resistor (R4) limits the current through M2.

Low-side Circuit Breaker

A low-side circuit breaker can be implemented if protection against excessive low-side currents is required. This low-side circuit breaker disconnects the ground connection to all ports. See Figure 56.

The LTC4296-1 low-side circuit breaker controls the N-channel MOSFET (M4) gate-to-source voltage with the LGATE and LSRC pins. M4 is fully enhanced when the first port enters the IDLE state. Low-side current is monitored with the voltage across sense resistor R2 measured at the LSNSn and OUTMn pins. Ports 1 and 2 share the LSNS1/2 sense pin, and ports 3 and 4 share the LSNS3/4 sense pin. A low-side current causing any of the low-side sense resistor voltage to exceed ΔV_{LSNS_FCBn} for t_{LSNS_FAULT} trips the circuit breaker; all LTC4296-1 ports that are out of the DISABLED state are forced to the OVERLOAD state.

Each port's low-side sense resistor R2 sets the low-side circuit breaker current threshold for that port. This current threshold should be set for over 50% higher than the high-side ACL threshold for the corresponding port. Use Equation 6 for calculating the value for R2 where I_{CB} is the circuit breaker current threshold.

$$R2 = < \Delta V_{LSNS\_FCBn(MIN)}/I_{CB} \text{ (Ω)} \quad (6)$$

Appropriate wattage should be selected for the sense resistors per Equation 7. It is good practice to select a power rating for at least double the resistor application power.

$$P_{R2} > 2 \bullet (\Delta V_{LSNS\_FCBn(MAX)})^2/R2 \text{ (W)} \quad (7)$$

Refer to the Layout Guidelines section for proper Kelvin Sensing with the sense resistor.

Figure 57 provides recommended R2 resistor values and power ratings per maximum port power class. Refer to the layout guidelines for proper Kelvin sense layout with the low-side sense resistor.

The low-side circuit breaker MOSFET must have an adequate V_{DS} rating for the maximum system application and fault conditions. Since this MOSFET is for fast circuit breaking and not current limiting, high SOA is not required compared to the high-side MOSFET. Low $R_{DS(ON)}$ helps minimize losses.

An internal switch from LSNS0 to GND establishes a return path for all the OUTMn pins to ground when the low-side MOSFET is disabled, e.g. DISABLED or DEEP SLEEP. RSLP_LSNS0 is the on resistance for deep sleep return. The deep sleep return switch is always on unless the low-side circuit breaker trips or an overcurrent fault occurs and will turn back on after a restart delay.

MDI FAULT TOLERANCE

Most applications with isolation will only require the high-side circuit breaker as shown on the front page application circuit. For applications requiring MDI fault tolerance from an external, positive or negative, forced voltage at the MDI, Figure 57 provides a protection solution.

APPLICATIONS INFORMATION

A rectifying circuit or device before the IN pin protects components at the supply from a positive backfeed voltage greater than the supply voltage.

The low-side circuit breaker, a low-side snubber (C9 and R9), a current steering diode (D2), and a TVS (D1) protect the PSE from negative voltages at the MDI. When a forced negative voltage is applied, D2 provides a return path for the low-side current through M4. When the low-side circuit breaker trips, M4 is open and capacitor C10 absorbs the inductive kickback. D2 continues to conduct until the snubber is charged to the forced negative voltage. High voltage ringing at LSNSn is steered by D3 to the TVS D1. The port is held in the OVERLOAD state during this fault.

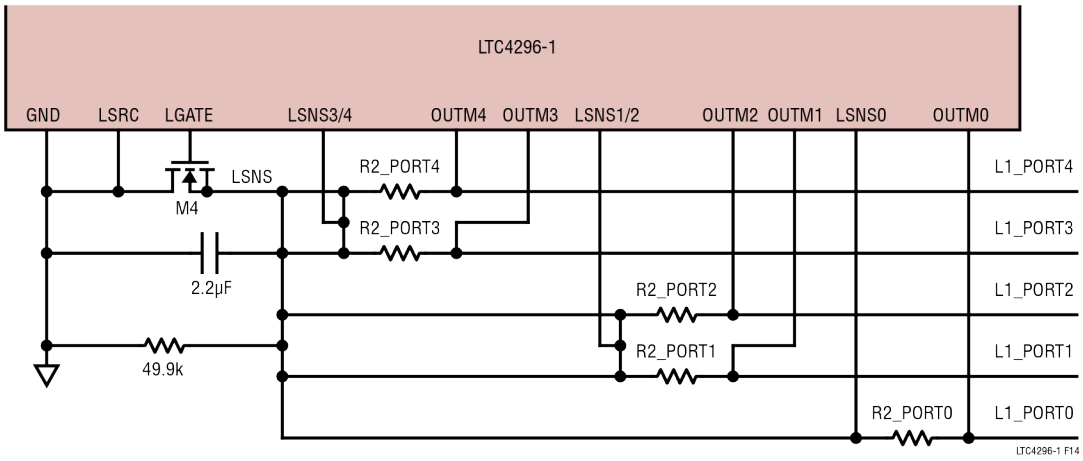
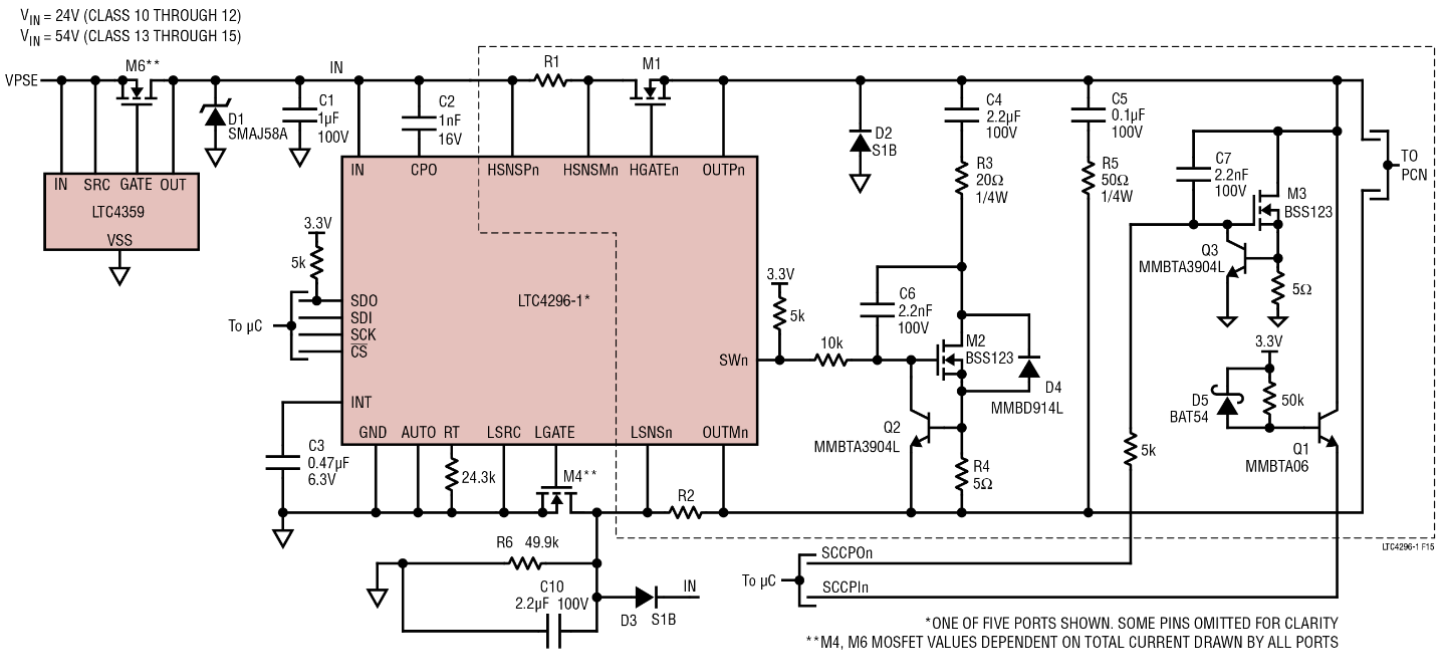


Figure 56. Low-Side Circuit Breaker

APPLICATIONS INFORMATION



IEEE 802.3cg PSE CLASS	HIGH-SIDE SENSE RESISTOR (R1)	LOW-SIDE SENSE RESISTOR (R2)	HIGH-SIDE MOSFET (M1)
CLASS 10	1.6Ω, 1/10W	0.4Ω, 1/10W	PSMN075-100MSE
CLASS 11	0.62Ω, 1/10W	0.16Ω, 1/10W	
CLASS 12	0.24Ω, 1/4W	0.062Ω, 1/4W	
CLASS 13	0.68Ω, 1/10W	0.180Ω, 1/10W	
CLASS 14	0.27Ω, 1/4W	0.068Ω, 1/4W	
CLASS 15	0.1Ω, 1/2W	0.025Ω, 1/4W	PSMN040-100MSE

Figure 57. LTC4296-1 PSE Port with MDI Fault Tolerance

LAYOUT GUIDELINES

Refer to the EVAL-LTC4296-1-AZ/BZ demo board as a layout reference. Standard power layout guidelines apply to the LTC4296-1, such as placing the decoupling caps for the IN, V_{INT}, and CPO supplies near their respective supply pins, use of ground planes, and use of wide traces wherever there are significant currents.

Kelvin Sense

Kelvin sense connections to the current sense resistors should always be used to ensure the specified current threshold accuracy is achieved. Figure 58 shows an example of proper Kelvin sensing for the high-side sense pins HSNSPn and HSNSMn to the respective sense resistor.

For applications that implement the optional low-side circuit breaker, care must be taken to minimize stray currents at the shared Kelvin signal LSNS1/2 between ports 1 and 2, and LSNS3/4 between ports 3 and 4. The OUTM1, OUTM2, OUTM3, and OUTM4 pins must also have proper Kelvin sense to the respective sense resistor. See Figure 59.

For the LSNS0 and OUTM0 signals, use the same Kelvin sense technique as shown for HSNSPn and HSNSMn in Figure 58.

DATA CONVERTERS

Internal Temperature Sensor

The internal junction temperature can be measured by programming the Global ADC Configuration register to select temperature sensor as the ADC input and enable the ADC for single-shot or continuous mode measurement (**gadccfg.gadc_sel** and **gadccfg.gadc_sample_mode**, respectively). The ADC results are available in the Global ADC Data register when the measurement is completed (**gadcdat.gadc**) after approximately 3.6ms and is updated every 1.8ms thereafter in continuous mode. The LTC4296-1 sets the GADC New Data bit (**gadcdat.gadc_new**) when the new measurement is available to read. The junction temperature (T_J) readout in °C can be determined by the following equation:

$$T_J\,(°C) = \frac{gadcdat.gadc - 2048}{4} - 273.15 \qquad (8)$$

APPLICATIONS INFORMATION

Port High-Side Current Readback

The port high-side current sense resistor voltage can be measured by reading the Port ADC result register (**pnadcdat.source_current**) while in the POWER_UP and POWER_ON states. The port ADC result register is updated every 1.8ms. The expression for the source current (I_{SOURCE}) readout as a function of the high-side current sense resistor (R1), can be determined by the following equation:

$$I_{SOURCE}\ (A) = \frac{(pnadcdat.source\_current - 2048) \bullet 10}{R1} \quad (9)$$

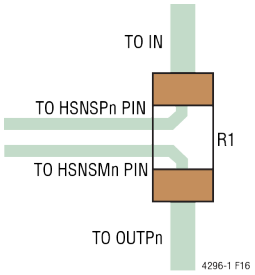


Figure 58. HSNSPn and HSNSMn Pin Kelvin Connection

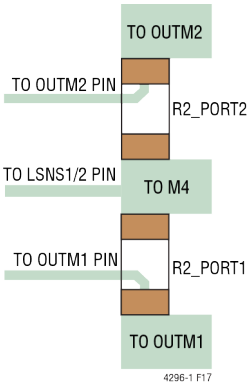


Figure 59. Shared LSNS1/2, OUTM1 and OUTM2 Pins Example Kelvin Sense Layout

Port Low-Side Current Readback

The port low-side current (I_{RETURN}) sense resistor voltage can be measured by programming the Global ADC Configuration register to select a port low-side current as the ADC input and enable the ADC for single-shot or continuous mode measurement (**gadccfg.gadc_sel** and **gadccfg.gadc_sample_mode**, respectively). The ADC results are available in the Global ADC Data register when the measurement is completed (**gadcdat.gadc**) after approximately 3.6ms and are updated every 1.8ms thereafter in continuous mode. The expression for current as a function of the high-side current sense resistor (R2) can be determined by the following equation:

$$I_{RETURN}\ (A) = \frac{(gadcdat.gadc - 2048) \bullet 100\mu V}{R2} \quad (10)$$

Input And Port Output Voltage Readback

The input voltage (V_{IN}) and port output voltage (V_{PORT})can be measured by programming the Global ADC Configuration register. Select input voltage V_{IN}, or port output voltage (V_{PORT} = V_{OUTPn}-V_{OUTMn}) as the ADC input and enable the ADC for single-shot or continuous mode measurement (**gadccfg.gadc_sel** and **gadccfg.gadc_sample_mode**, respectively). High-gain or low-gain resolution may be selected in continuous mode. The ADC results are available in the Global ADC Data register when the measurement is completed (**gadcdat.gadc**) after approximately 3.6ms and is updated every 1.8ms thereafter in continuous mode. The expression for input and port output voltage can be determined by the following equations:

$$\begin{aligned} &\text{Low-Gain} \\ &V_{IN}(V),\ V_{PORT}(V) = \\ &(gadcdat.gadc - 2048) \bullet 35.2mV \\ &\\ &\text{High-Gain} \\ &V_{IN}(V),\ V_{PORT}(V) = \\ &(gadcdat.gadc - 2048 \bullet 17.6mV \end{aligned} \quad (11)$$

ISOLATION CONSIDERATIONS

Traditional IEEE 802.3 multi-pair Ethernet specifications require that network segments (including PoE circuitry) be electrically isolated from the chassis ground of each network interface device. However, IEEE 802.3bu (PoDL) and IEEE 802.3cg (SPoE) only require that the PD provides at least 1 MΩ isolation between all accessible external conductors and the MDI, when measured using 5V ± 20%. Both of these standards also require that all equipment comply with local, state, national, and application specific standards, such as the applicable sections of IEC 61010-1 or IEC 62368-1:2018.

For simple devices with no electrically conducting pins other than the twisted-pair Ethernet MDI, the isolation requirement can be met by using a non-conductive chassis enclosure.

For SPoE applications that require galvanic isolation from chassis, an isolated power supply must be used to power the LTC4926-1 and SPoE. Any I/O crossing the isolation must have some form of high-voltage tolerant coupling. Proper layout techniques must be implemented to maintain the high-voltage isolation on the PCB.

LOW-DROOP APPLICATIONS

Figure 60 shows a high-current application circuit suitable for applications where the PHY transmitter droop requirement is 10% as opposed to the 25% requirement for IEEE 802.3cg.

APPLICATIONS INFORMATION

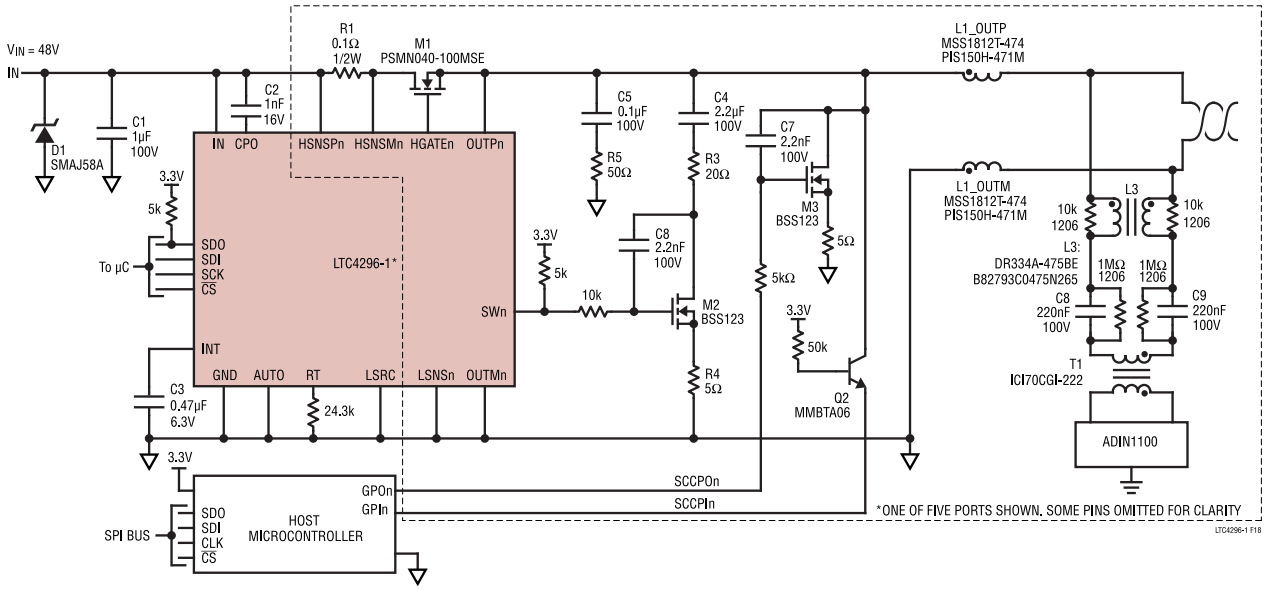
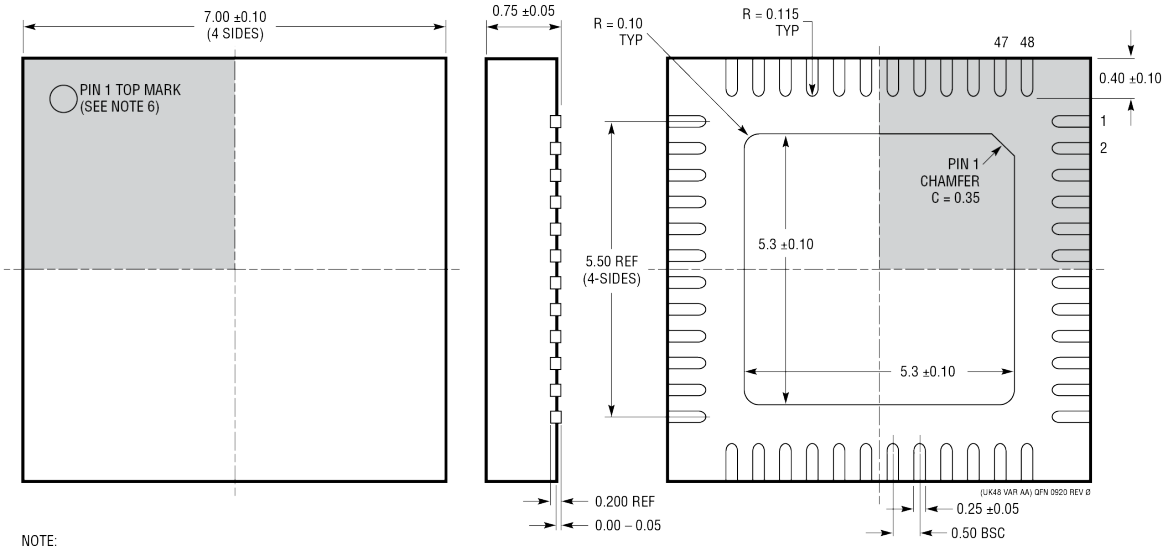


Figure 60. High-Current, Low-Droop Application Circuit

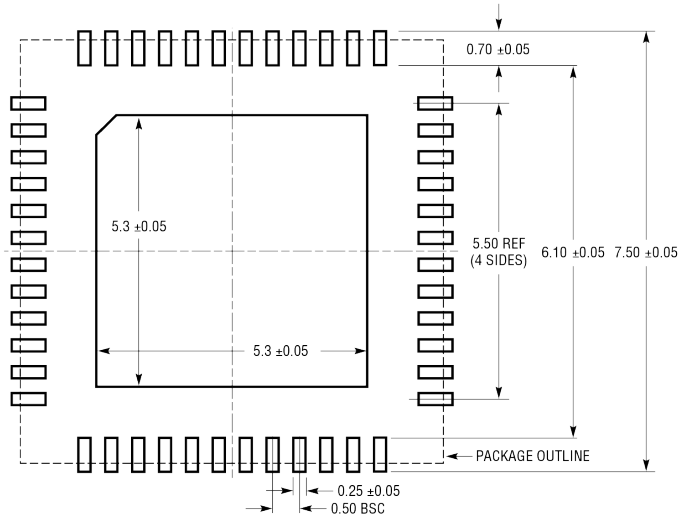
PACKAGE DESCRIPTION

UK Package
48-Lead Plastic QFN (7mm × 7mm)
(Reference LTC DWG # 05-08-7073 Rev Ø)
Exposed Pad Variation AA



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WKKD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

BOTTOM VIEW—EXPOSED PAD



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

TYPICAL APPLICATION

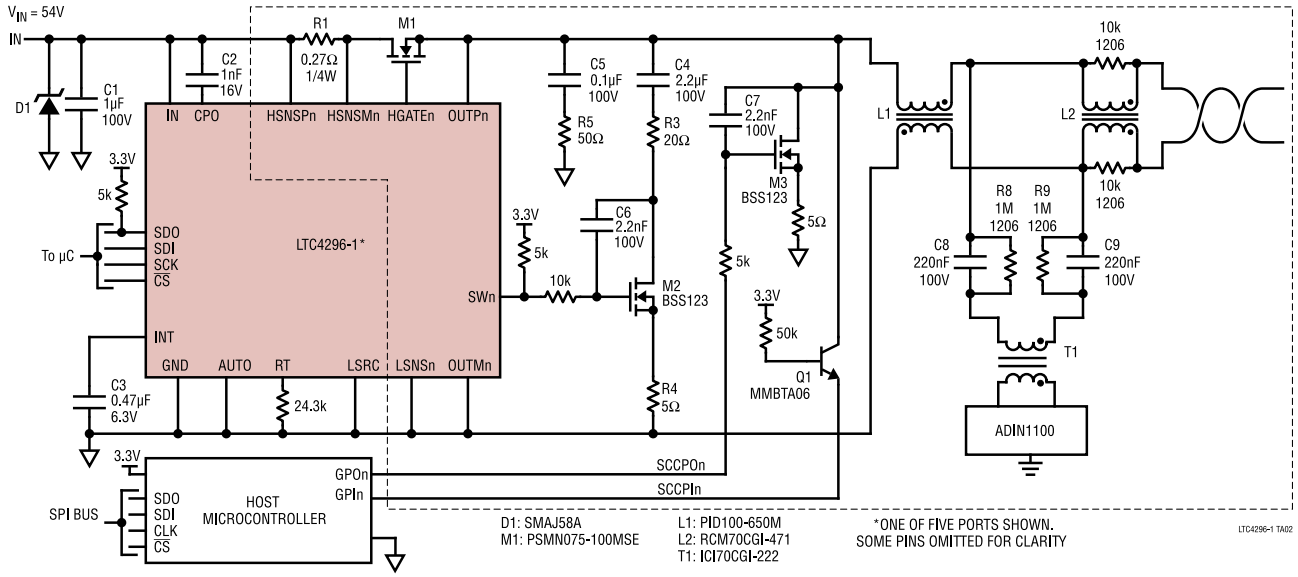


Figure 61. IEEE 802.3cg Class 14 PSE

RELATED PARTS

Table 21.

PART NUMBER	DESCRIPTION	COMMENTS
LTC9111	IEEE 802.3cg SPoE PD Controller	IEEE 802.3cg Compliant, Supports SCCP, External Switch, Low-Side Ideal Bridge, Pin Programmable Class Configuration, 2.3V to 60V Input Range
ADIN1100	Robust, Industrial, Low Power 10BASE-T1L PHY	Low Power, Single Port Transceiver; Compliant with IEEE 802.3cg-2019 Ethernet Standard for Long Reach SPE
ADIN1110	Robust, Industrial, Low Power 10BASE-T1L Ethernet MAC-PHY	Ultralow Power, Single Port Transceiver; Compliant with IEEE 802.3cg-2019 Ethernet Standard for Long Reach SPE
ADIN2111	Low Complexity, 2-Port Ethernet Switch with Integrated 10BASE-T1L PHYs	Low Power, Low Complexity, Two-Ethernet Ports Switch and One SPI Port
LTC4359	Ideal Diode Controller with Reverse Input Protection	4V to 80V Operation, –40V Reverse-Input Protection, Low 13µA Shutdown Current
LT8641	65V, 3.5A Synchronous Step-Down Silent Switcher® with 2.5µA Quiescent Current	$V_{IN(MIN)}$ = 3V, $V_{IN(MAX)}$ = 65V, $V_{OUT(MIN)}$ = 0.81V, I_Q = 2.5µA, ISD < 1µA, 3mm × 4mm QFN-18
LTC3630A	6V, 500mA Synchronous Step-Down DC/DC Converter	V_{IN}: 4V to 76V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 12µA, ISD = 5µA, 3 × 5 DFN-16, MSOP-16(12)E
LT8301	42V_{IN} Micropower Isolated Flyback Converter with 65V/1.2A Switch	Low I_Q Monolithic No-Opto Flyback 5-Lead TSOT-23
ADUM1251	Hot Swappable, Dual I^2C Isolators	Bidirectional I^2C communication, 1000 kHz operation, Suitable for Hot Swap Applications
ADUM162N	Robust 3.0 kV rms Six Channel Digital Isolators w/Fail-Safe and 2 Reverse Channels	Low Propagation Delay, 150 Mbps Maximum Guaranteed Data Rate