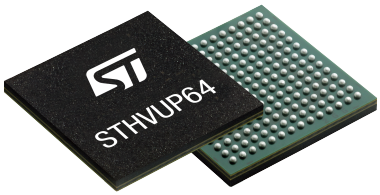
STHVUP64

Databrief

64 channels ±100 V, ±0.2/0.4 A, 3/5-level RTZ, TR switch, high-speed ultrasound pulser with integrated transmit beamformer



Product status link
STHVUP64

Product summary	
Order code	STHVUP64
Package	FCBGA196 10X10X1.4
Packing	Tray

Product label
SUSTAINABLE TECHNOLOGY

Features

- 0 to 200 V output signal peak-to-peak
- Gate drivers self-biased architecture, no filtering capacitors required
- Pulsed wave (PW) and continuous wave (CW) mode operations:
  - 3 or 5-level output waveform
  - High Impedance state
  - Programmable ±200 mA or ±400 mA source and sink current in 3-level configuration
  - ±200 mA source and sink current in 5-level configuration
- Fully integrated real clamping-to-ground function
  - 45 Ω clamp resistance
- Fully integrated transmitting/receiving switches (TR_SW)
  - 45 Ω ON-resistance
  - 18 pF ON-capacitance
  - 3 pF OFF-capacitance at LVOUT pin
  - Compliant with receiver multiplexing function
- Auxiliary integrated circuits
  - Noise blocking diodes
  - Thermal protection
  - Undervoltage protection and bias supply checks
- Programmable power management to optimize the performances in case of ultra-portable applications
- Beamforming in transmission mode
  - Programmable single channel delay for beam steering and beam focusing
  - Clock frequency up to 200 MHz
  - 5 ns delay resolution
  - From 5 ns to 20 us delay range @ 200 MHz
  - 3 us minimum delay table writing time
- Embedded memory to store transmission patterns
  - 32 states for waveform definition
  - Waveform compression algorithm
- Easy driving control
  - Control through standard Quad Serial Peripheral Interface (QSPI)
  - Few input signals to drive several devices
  - Single Interrupt as alert signal
  - Single Trigger to manage transmitting (TX) and receiving (RX) phases, fully automatic and programmable
  - Anti-glitch on trigger signal during TX phase
- Checksum control
- Very low package thermal resistance
- Latch-up free due to HV SOI technology
- Just a few passive components needed
- Small package: BGA 10mm x 10mm with 196 balls and 0.65mm pitch

Application

- Medical ultrasound imaging
- Pulse waveform generators
- Ultra-portable ultrasound imaging
- Piezoelectric transducer drivers

Description

The STHVUP64 is monolithic, high-voltage and high-speed pulse generator features 64 independent channels integrating a 64-channel beamformer for pulse generation in multi-channel medical ultrasound applications targeted at low power ultra-portable system.

A pure analog section provides each channel two half-bridges (two high-voltage P-channel and two high-voltage N-channel MOSFETs), a clamping-to-ground circuit and a transmitting/receiving switch structure which guarantees an effective isolation during the transmission phase. Each channel features also integrated high-voltage level translators, noise blocking diodes and an anti-leakage circuit.

Through a dedicated bit, channels can be programmed as a 3-level output or as a 5-level output. In 3-level mode, the two half-bridges are driven in parallel to provide a default peak current of 400 mA. However, it is also possible to program a low-consumption mode to decrease the overall power consumption: in this case, only one half-bridge is used and the output current lowers down to 200 mA. In 5-level mode, the two half-bridges can be driven independently, and each half-bridge has a current capability of 200 mA. The clamp circuit, used to force the XDCR<63:0> output pins down to GND, has a resistance of 45 Ω and a peak current capability of 0.32 A. The 64 independent T/R switches can be used in a multiplexing configuration.

The STHVUP64 also includes some global blocks: thermal protection circuits, undervoltage checks on VDDP3V3, VDDM3V3 and DVDD, a power-on-reset (POR) on DVDD and a global self-biased high-voltage MOSFET gate driver with internal check of the correct value and of the HV supplies.

All functions are managed by a digital core working at a maximum clock frequency of 200 MHz. This block manages the delay profiles used in the beamformer, the waveform generation and the various global settings and grants that all the device operations are performed in the correct sequence.

Revision history

Table 1. **Document revision history**

Date	Version	Changes
04-Aug-2022	1	Initial release.

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