TDA38640 OptiMOS iPOL

40A Single-voltage Synchronous Buck Regulator with SVID and I2C

Quality Requirement Category: Industrial

Features

- Single 4.5V to 17V application or Wide Input Voltage Range from 3.0 V to 17 V with external Vcc
- Output Voltage Range: 0.25V to 3.04 V with external feedback resistor divider
- Enhanced Stability Engine Stable with Ceramic Capacitors and no External Compensation
- Optional Forced Continuous Conduction Mode and Diode Emulation for Enhanced Light Load Efficiency
- Programmable Switching Frequency from 400 kHz - 2 MHz in steps of 200 kHz, excluding 1600 kHz
- Monotonic Start-Up with Selectable Soft-Start Time & Enhanced Pre-Bias Start-Up
- Thermally Compensated Internal Over-Current Protection with Eight Selectable Settings
- I2C system interface for reporting of Temperature, Voltage, Current & Power telemetry
- Multiple Time Programming (MTP) with up to 24 writes for the USER section
- Digitally programmable load-line no external components are needed
- Thermal Shut Down
- Operating temp: -40°C < Tj < 125°C
- Small Size: 5mm x 6mm PQFN
- Lead-free, Halogen-free and RoHS2 Compliant with Exemption 7a

Applications

- Server Applications
- Storage Applications
- Telecom & Datacom Applications
- Distributed Point of Load Power Architectures

Description

The TDA38640 is an easy-to-use, fully integrated and highly efficient DC/DC regulator.

The onboard PWM controller and OptiMOS™ FETs with integrated bootstrap diode make TDA38640 a small footprint solution, providing high-efficient power delivery.

TDA38640 is a versatile regulator, operating with wide input and output voltage range, offering eight programmable switching frequency from 400 kHz to 2MHz excluding 1600 kHz, and providing eight unique selectable current limits.

It also features important protection functions, such as pre-bias start-up, thermally compensated current limit, over voltage and under voltage protection, and thermal shutdown to give required system level security in the event of fault conditions. The device configuration can be easily defined using Infineon's PowerClient GUI and is stored in the on-chip memory. The TDA38640 provides extensive OVP, UVP, OCP, OTP & Boot UVLO fault protection. The controller requires the fewest possible external components and resulting in a simplified Bill of Materials (BOM).
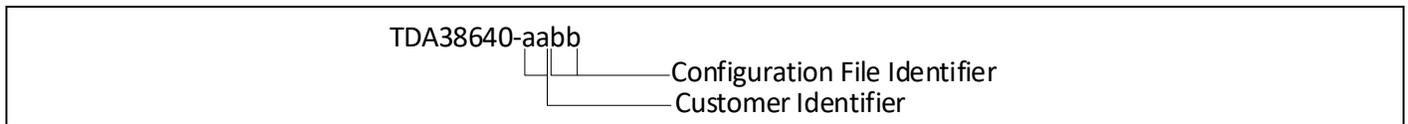
Table of Contents

1 Ordering Information

Table 1   Ordering Information

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form and Qty		
TDA38640	QFN 5mm x 6mm	Tape and Reel	TBD	TDA38640aabbAUMA1

TDA38640-aabb
Configuration File Identifier
Customer Identifier

Figure 1   Orderable Part Number Description
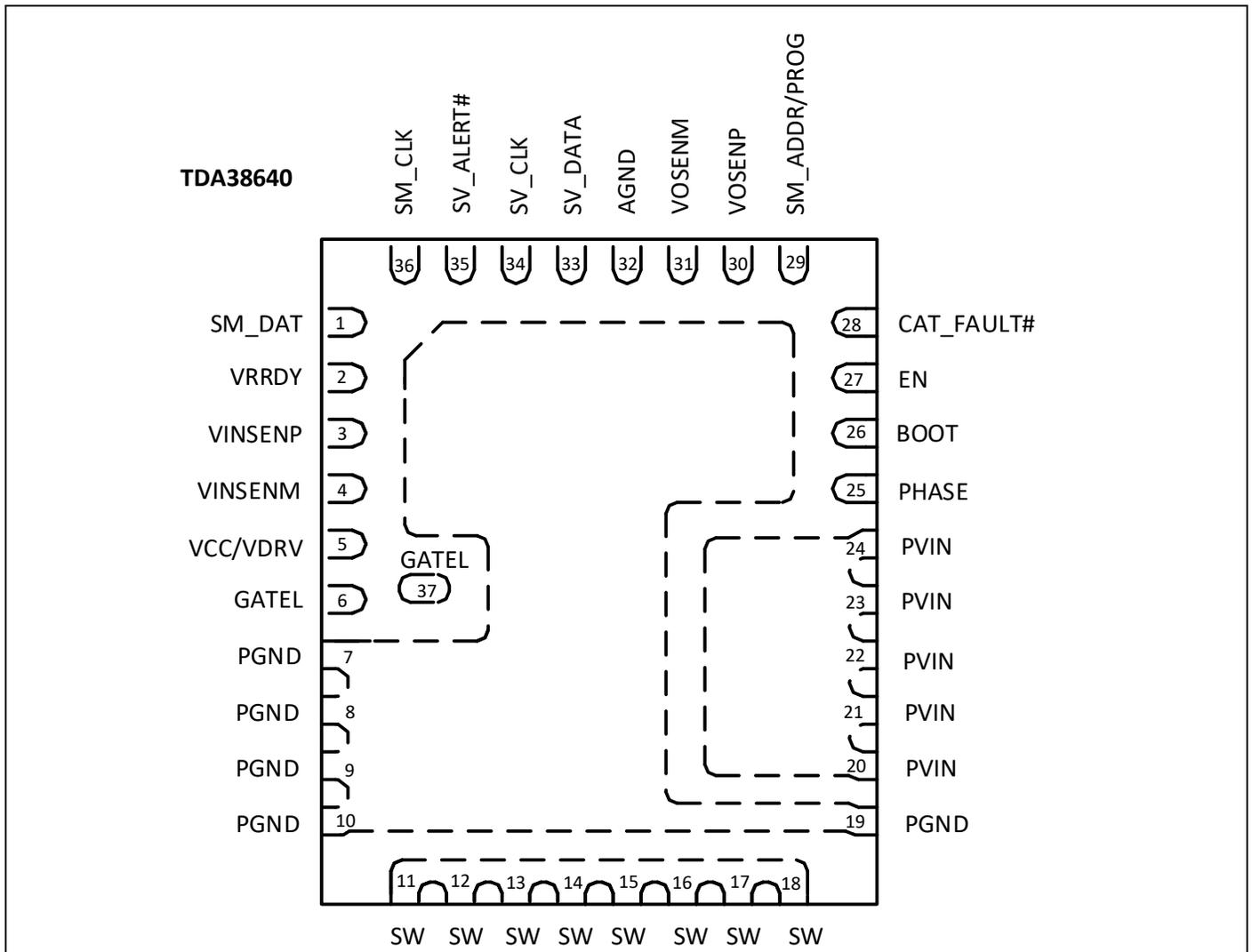
Figure 2   Package Top View

2 Functional Block Diagram
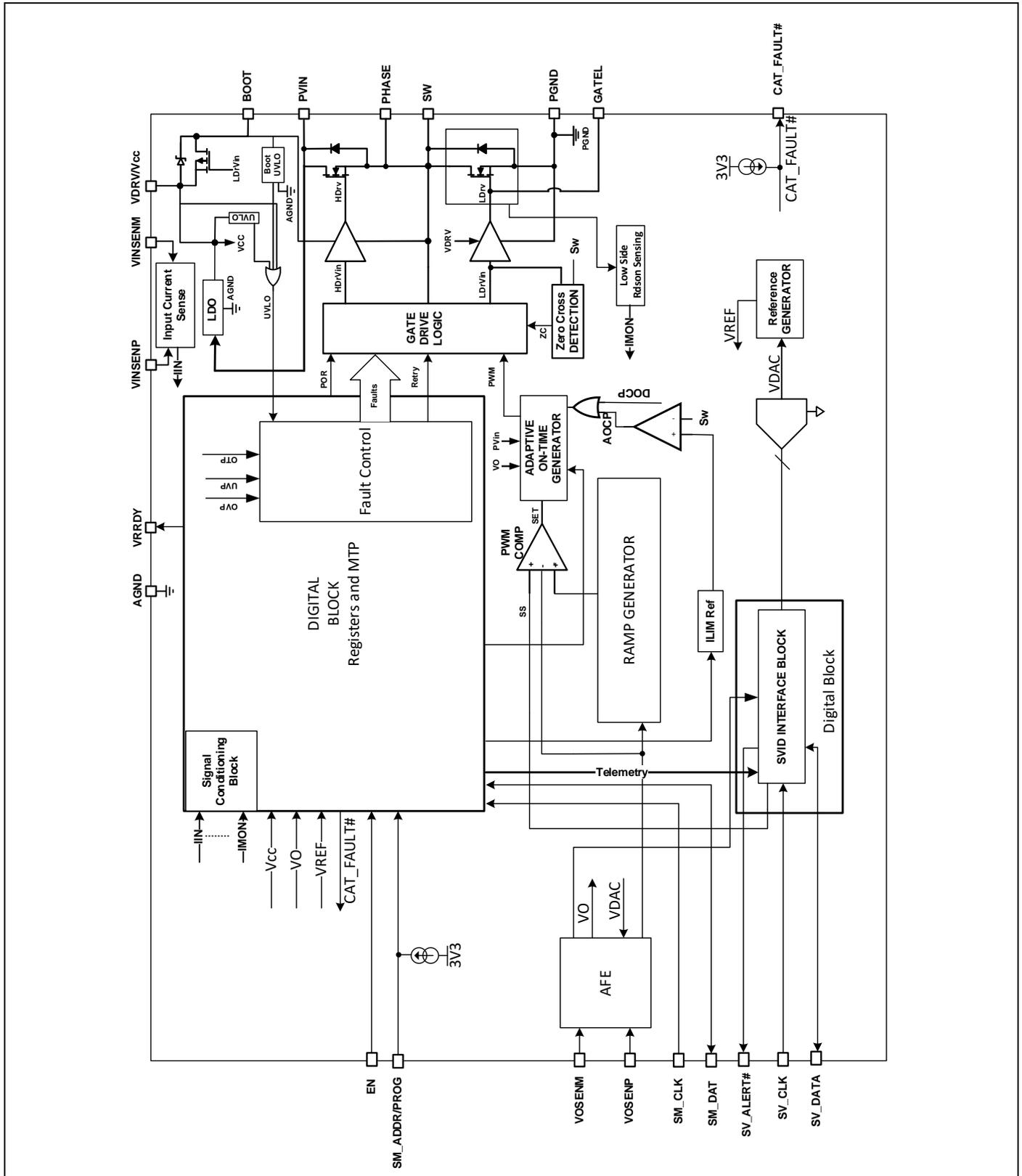
Figure 3   Block Diagram

3 Typical Application Diagram
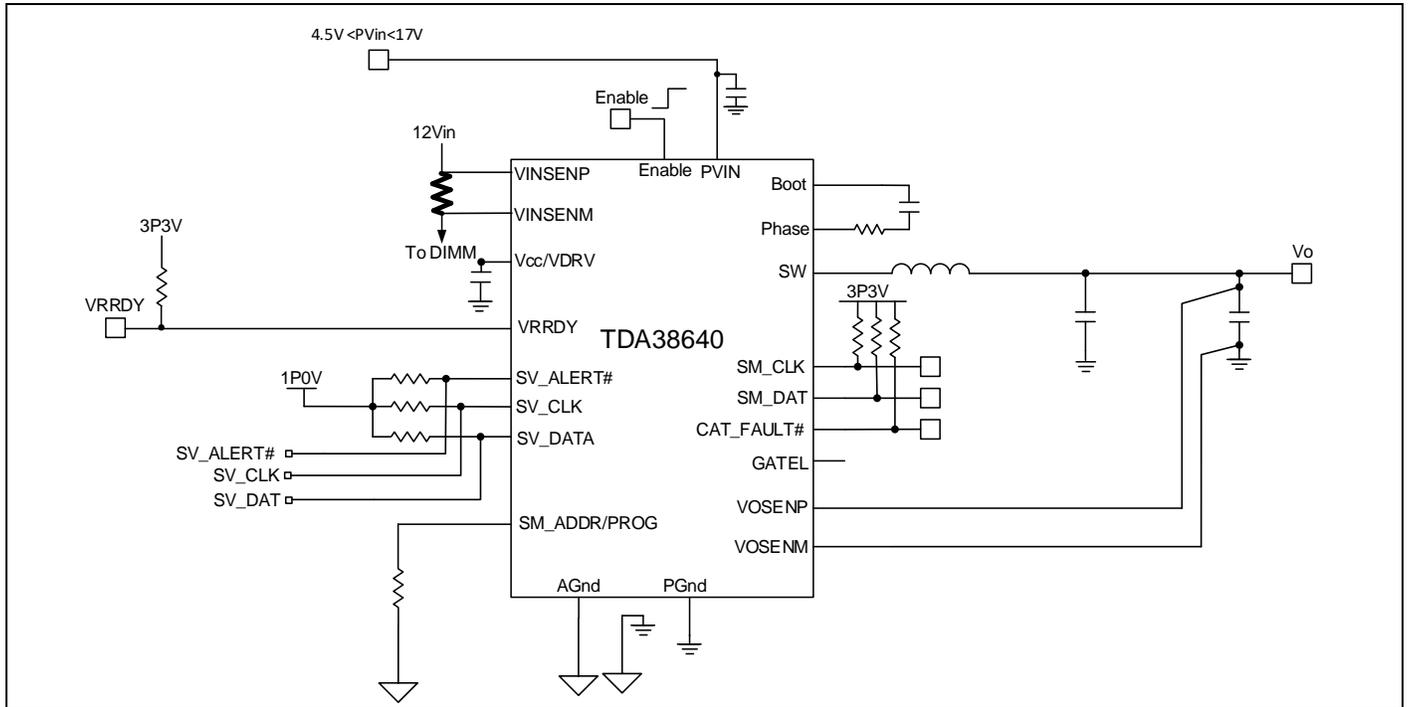
Figure 4 TDA38640 Basic application circuit with Input Current Sense Enabled (0.25 V ≤ VID ≤ 2.56 V)
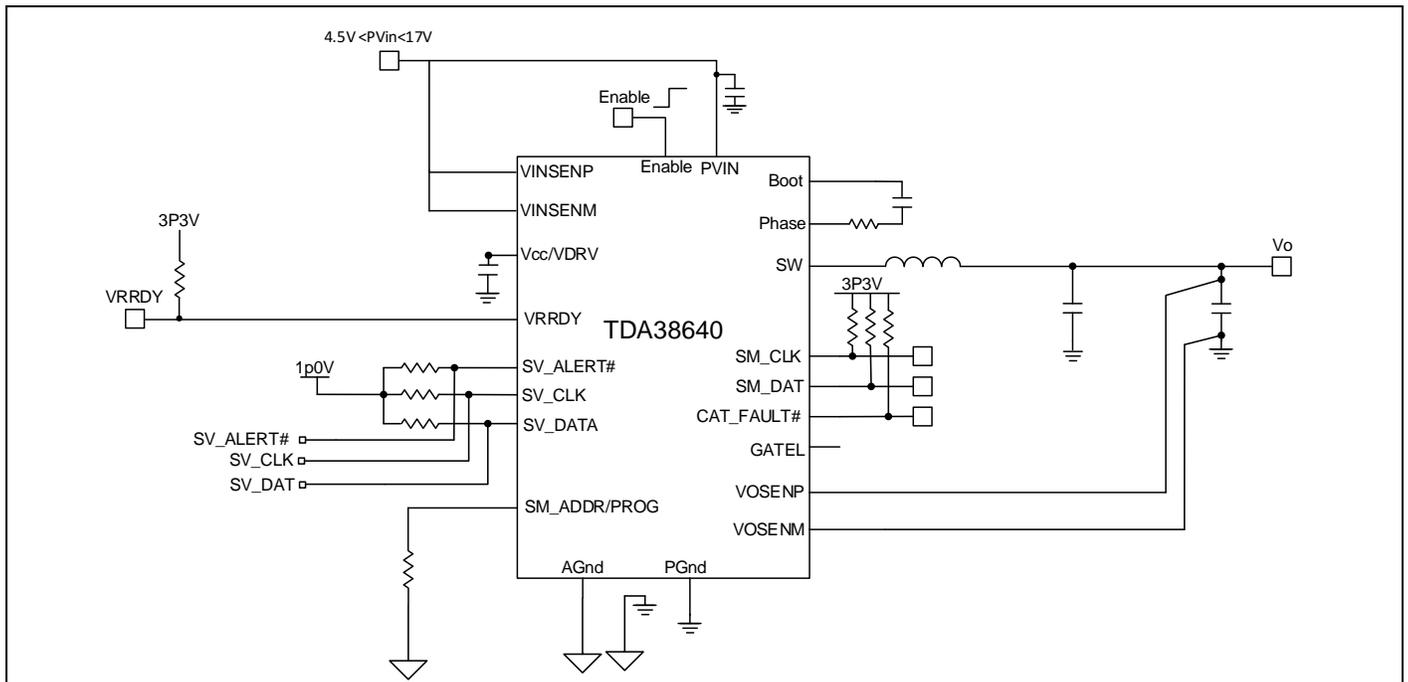
Figure 5 TDA38640 Application Circuit with Input Current Sense Disabled (0.25 V ≤ VID ≤ 2.56 V)

Infineon

4 Pin Descriptions

Table 2 Pin Descriptions

Note: A- Analog; D- Digital; [I]- INPUT; [O]- OUTPUT; [B]- BI-DIRECTIONAL; [P]- POWER

Pin#	Pin Name	Pin Type	Pin Description
1	SM_DAT	D [B]	I2C bi-directional serial data line. Ground if not used.
2	VRRDY	D [O]	Open-drain output that asserts high when the VR has completed soft-start to boot. Pull-up to an external voltage through a resistor.
3	VINSENP	A [I]	This pin connects to the positive side of the shunt resistor that is used to monitor the input current.
4	VINSENM	A [I]	This pin connects to the negative side of the shunt resistor that is used to monitor the input current.
5	Vcc/Vdrv	A [P]	Input bias for the external Vcc voltage/output of the internal LDO and internal driver. A 2.2uF ceramic capacitor is recommended to use between Vcc and the Power ground (AGND).
6, 37	GATEL	A [O]	Gate of Low-side FET. The signal on this pin should be used for test purposes only and should not have external components connected to it.
7, 8, 9, 10, 19	PGND	-	Power Ground. Should be connected to the system's power ground plane. PGND and AGND are internally connected via the lead frame.
11, 12, 13, 14, 15, 16, 17, 18	SW	A [O]	Switch Node. Connect these pins to an output inductor.
20, 21, 22, 23, 24	PVin	A [P]	Input supply for the power stage.
25	Phase	A [O]	Source of High-side FET. Connect a bootstrap capacitor between this pin and Boot pin. A high temperature (x7R) 0.1uF or greater value ceramic capacitor is recommended.
26	Boot	A [I]	Supply voltage for the high side driver. Connect this pin to the Phase pin of the regulator through a bootstrap capacitor. For PVin above 14V, a resistor is recommended in series with the bootstrap capacitor to control the slew rate of the SW node rising edge.
27	EN	A [I]	Enable pin to turn on and off the IC.
28	CAT_FAULT#	D [O]	This is an Active Low open drain output that asserts when a catastrophic fault is detected.
29	SM_ADDR/PROG	D [I]	I2C Slave Address. A resistor to ground on this pin points to one of the unique 16 I2C slave devices which needs to be addressed on the board. It also provides access to the multi-configuration's by adding a fixed offset to the I2C slave address. The same address also defines the specific configuration file that will be loaded into the OTP during power-up

Pin Descriptions

Pin#	Pin Name	Pin Type	Pin Description
30	VOSENP	A [I]	Direct sense output line connected after the switch node inductor.
31	VOSENM	A [I]	This pin provides the return connection for a remote output voltage sensing. It is used as the internal reference voltage by the Analog Front End (AFE).
32	AGND	-	Signal ground for the internal circuitry
33	SV_DATA	D [B]	Serial VID Data I/O. Is a bi-directional serial line over which the CPU Master issues commands to controller/s slave/s and receives data back. Groud the pin if not being used.
34	SV_CLK	D [I]	Serial VID Clock Input. Clock input driven by the CPU Master. Groud the pin if not being used.
35	SV_ALERT#	D [O]	Serial VID ALERT# (INTEL). SV ALERT# is pulled low by the controller to alert the CPU of VR 14/13/12/12.5 status. Pull-up to an external voltage through a resistor.
36	SM_CLK	D [I]	Serial Clock Line Input. I2C clock input. The interface is rated to 1 MHz. Groud the pin if not being used.

5 Absolute Maximum Ratings

Table 3   Absolute Maximum Ratings

PVin, VINSENP (Note 1)	-0.3 V to 25 V
VINSENM	-0.3 V to 25 V
En to PGND	-0.3 V to 6 V
PVin to Phase and SW	-0.3 V to 25 V(DC), below -5 V for 5 ns and 32 V for 2 ns
Vcc to PGND (Note 1)	-0.3 V to 6 V
GATEL to PGND (Note 1)	-0.3 V to 6 V
Boot to PGND (Note 1)	-0.3 V to 25 V(DC), below -0.3 V for 5 ns and 31 V for 10 ns
SW and PHASE to PGND (Note 3)	-0.3 V to 25 V (DC), below -5 V for 5 ns and 32 V for 2 ns
PVin to PHASE	-0.3 V to 25 V(DC), below -5 V for 5 ns and 32 V for 2 ns
Boot to Phase	-0.3 V to 6 V (DC), 7 V for 5 ns
SM_ADDR/PROG, VOSENP, and VRRDY to PGND (Note 1)	-0.3 V to 3.6 V
PGnd to AGND	-0.3 V to +0.3 V
VOSENM to AGND	-0.3 V to +0.3 V
Storage Temperature Range	-55°C to 150°C
Junction Temperature Range	-40°C to 150°C

Note:

1.   *PGND and AGND pins are connected together*

Attention: ***Stresses beyond these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.***

6 Thermal Characteristics

Table 4   Thermal Characteristics

Description	Symbol	Values	Test Conditions
Junction to Ambient Thermal Resistance	θ_{JA}	19 °C/W	Note 2
Junction to PCB Thermal Resistance	$\theta_{JC\text{-}PCB}$	1.1 °C/W	Note 3
Junction to Case Top Termal Resistance	θ_{JC}	24 °C/W	

Note:

2. *Thermal resistance is measured with components mounted on a standard EVAL_TDA38640_1Vout demo board in free air*

3. *Thermal resistance is based on the board temoerature near pin 22*

7 Electrical Specifications

Table 5 Recommended Operating Conditions for Reliable Operation with Margin

Description	Min	Max	Unit	Note
PVin Voltage Range with External Vcc	3	17	V	Note 4, Note 5
PVin Voltage Range with Internal LDO	4.5	17	V	Note 5 , Note 6 & Note 10
Vcc Supply Voltage Range	4.3	5.5	V	Note 4 , Note 7
Output Voltage Range	0.25	3.04	V	Note 8
Continuous Output Current Range		40	A	Note 9
Switching Frequency (excluding 1600 kHz)	400	2000	kHz	Note 10
Operating Junction Temperature	-40	125	°C	

Note:

4. *VCC/VDRV pin is connected to an external bias voltage for PVIN less than 4.5 V*

5. *A common practice is to have 20% margin on the maximum SW node voltage in the design. For applications requiring PVin equal to or above 14V, a small resistor in series with the Boot pin should be used to ensure the maximum SW node spike voltage not exceeding absolute maximum DC and AC specs. Alternatively, a snubber can be used at SW node to reduce the SW node spike.*

6. *PV_{in} with internal LDO is used. For single-rail applications with the internal LDO and PV_{in} = 4.5 V-5.4 V, the internal LDO may enter dropout mode. AOCP limits can be reduced due to the lower VCC voltage.*

7. *The TDA38640 is designed to function with VCC down to 4.3 V, however, electrical specifications such as AOCP limits may be degraded.*

8. *The maximum output voltage is limited by the minimum off-time. For output voltages above 2.56 V an external feedback resistor divider is needed*

9. *Refer to Section x for maximum output current rating at different ambient temperatures.*

10. *The maximum LDO output current must be limited within 60 mA for operations requiring full operating temperature range of -40 °C ≤ T_J ≤ 125 °C. Figure 6 shows the maximum LDO output current capability over junction temoeraqture. Thermal De-rating may be needed at an elevated ambient tremperature to ensure the junction temperature within the recommended operating range.*

Electrical Specifications

7.1   Electrical Characteristics

Unless otherwise specified, these specifications apply over, 4.3V ≤ Vin = PVin ≤ 17V, in 0°C < T_J < 125°C. Typical values are specified at Ta = 25°C.

Table 6   Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Stage						
Top Switch	$R_{ds(on)\_Top}$	VBoot – Vsw= 5.0V, IO = 35A, Tj =25°C	-	2.9	-	mΩ
Bottom Switch	$R_{ds(on)\_Bot}$	Vcc = 5.0, IO = 35A, Tj =25°C	-	1.0	-	
Bootstrap Diode Forward Voltage		I(Boot) = 25mA	-	780	950	mV
SW Leakage Current	I_{SW}	SW = 0V, EN = 0V	-	-	175	µA
		SW = 0V, EN = high, No Switching	-	-	175	
Dead Band Time	T_{db}	SW Node rising edge, 40 A, Internal LDO, T_j=25C, Note 11	-	10	-	ns
		SW Node falling edge, 40 A, Internal LDO, T_j=25C, Note 11	-	10	-	
Supply Voltage	**PVin**					
PVin range (using external VCC = 5V)			-	3 - 17	-	V
PVin Range (using internal LDO)		Fsw = 600 kHz	-	4.3 – 17	-	V
		Fsw = 2 MHz	-	4.3 – 17	-	
Extrernal Vcc Range			4.5	5	5.5	V
Supply Current	**Iin**					
PVin Supply Current (standby)	$I_{in (Standby)}$	EN = Low, No Switching	-	12	-	mA
Digital Inputs	**VR_ENx (Intel)**					
Input High Voltage			0.70	-	-	V
Input Low Voltage			-	-	0.30	V
Input Impedance			-	1	-	MΩ
Digital Inputs	**SV_CLK, SV_DAT**					
Input High Voltage			0.65	-	-	V
Input Low Voltage			-	-	0.45	V
Hysteresis			-	95	-	mV
Input Leakage Curent		SV_CLK=3.6 V	-	-	±1	µA
Pin Capacitance		See Note 11	-	-	4	pF
Digital Inputs - LVTTL	**SM_DAT, SM_CLK**					
Input High Voltage			1.35	-	-	V

Electrical Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Low Voltage			-	-	0.8	V
Input Leakage		SM_CLK = 3.6 V	-	-	±1	µA
Pin Capacitance		See Note 11	-	-	4	pF
Remote Voltage Sense Inputs	**VOSENP, VOSENM**					
VOSENP Input Current		VOSENP = 3.6 V	-	-	230	µA
		VOSENP = -0.3 V	-85	-	-	µA
VOSENM Input Current		VOSENM = 0.3 V	-155	-	-	µA
		VOSENM = -0.3 V	-200	-	-	µA
Differential Input Voltage Range			-	-	2.56	V
VOSENM Input CM Voltage			-	±300	-	mV
Input Current Sense Input	**VINSENP, VINSENM**					
VINSENP Input current			-	200	-	µA
VINSEM Input Current			-	-	5	µA
Input Current Sense Accuracy			-	-	-	mV
Analog Address/Level Inputs	**SM_ADDR/PROG**					
Output Current			-	15	-	µA
CMOS Outputs – 3.3V	**CAT_FLT**					
Output High Voltage		Ioh = - 4 mA	Vcc-0.4	-	-	V
Ouptut Low Voltage		Ioh = 4 mA	-	-	0.4	V
Open-Drain Outputs–4mA Drive	**VRRDYx, CAT_FAULT#**					
Output Low Voltage		I = 4mA	-	-	0.3	V
Output Leakage		0 – 3.6 V	-	-	±5	µA
Open-Drain Outputs-20mA Drive	**SV_DAT,SV_ALERT#, SM_DAT**					
Output Low Voltage		I = 20 mA	-	-	0.26	V
On Resistance		I = 20 mA	7	9	13	Ω
Tri-State Leakage			-	-	±5	µA
On-Time Timer						
Frequency Range (programmable)		Excluding 1600kHz and in steps of 200 kHz	400	--	2000	kHz
Minimum On-Time		Note 11, Vin=12V, Vo=0V, See Note 11	-	25	-	ns
Minimum Off-Time	Toff (Min)	Tj=25°C, VFB=0 V, See Note 11	-	150	-	ns
System Set Point Accuracy (5 mV and 10 mV step mode voltage)						
VBOOT Voltage Range			Meets Spec			V
$0.25\,V \le VID \le 0.795\,V$		$-40°C \le T_J \le 125°C$	-	±8	-	mV
$0.8\,V \le VID \le 0.995\,V$		VDD > VID + 200 mV	-	±5	-	mV

Electrical Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
0.8 V ≤ VID ≤ 2.52 V		Typ = 3σ	-	±0.5	-	%VID
VCC LDO Output	**Vcc**					
Output Voltage	Vcc	5.5V ≤ Vin ≤ 17V, when Icc =50mA, Cload = 2.2uF, T_j=25C	4.7	5.0	5.3	V
VCC Dropout	Vcc_drop	Vin = 4.3V, Icc=50mA, Cload=2.2uF, T_j=25C	-	650	-	mV
Short Circuit Current	I_{short}	Vin = 12 V, T_j=25C	-	450	-	mA
Under-Voltage Lockout						
Vcc_Good Start Threshold	VCC_UVLO_Start	Vcc Rising Trip Level	3.8	-	4.0	V
Vcc_Good Stop Threshold	VCC_UVLO_Stop	Vcc Falling Trip Level	3.6	-	3.8	V
Enable-Start-Threshold	Enable_UVLO_Start	ramping up	0.61	0.65	0.69	V
Enable-Stop-Threshold	Enable_UVLO_Stop	ramping down	0.51	0.55	0.59	V
IMON Reporting Accuracy						
IMON Accuracy TDA38640 (40 A)	Imon	Maximum load	-	±6	-	%
Over Current Limit						
Current Limit Threshold (Valley Current)	I_{oc}	Tj = 25°C, Vcc =5.0V	-	10	-	A
			-	15	-	
			-	20	-	
			-	25	-	
			-	30	-	
			-	40	-	
			-	50	-	
			-	60	-	
Current Limit Threshold Accuracy		See Note 11	-20	-	20	%
Over-Voltage Protection						
Output Fixed OVP Threshold (Programmable)	OVP_Vth	VID Rising	-	0.8	-	V
			-	1.0	-	
			-	1.2	-	
			-	1.35	-	
			-	1.5	-	
			-	1.8	-	
			-	2.2	-	
			-	2.85	-	
Output Fixed OVP Threshold Accuracy			-	±5	-	%
Output Relative OVP Threshold (programmable)		Relative to VID in steps of 50 mV	50	-	400	mV
Output Relative OVP Threshold Accuracy		Relative to VID in steps	-25	-	25	mV

Electrical Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Under-Voltage Protection						
Output Relative UVP Threshold (programmable)	UVP_Vth	Relative to VID in steps of 50 mV	50	-	400	mV
Output Relative UVP Threshold Accuracy		Relative to VID is steps	-	±25	-	mV
I2C and Reporting						
Bus Speed		Normal	-	100	-	kHz
		Fast	-	400	-	kHz
		High-Speed	-	1000	-	kHz
Output Voltage Resolution			-	0.244, 1.953, 3.906	-	mV
Output Voltage Filter Rate			-	8	-	kHz
Output Voltage Update Rate			-	379	-	kHz
Highest Reported Vout		VOUT_SCALE_LOOP=1	-	2.5	-	V
Vout Reporting Accuracy		-40°C-125°C (Tj), 4.5V<Vcc<5.5V	-1	-	1	%
Iout Resolution			-	0.0625	-	A
Iout Filter Rate			-	8	-	kHz
Iout Update Rate			-	379	-	kHz
Iout Digital Monitoring Range			-		40	A
Iout Reporting Accuracy (PMBus)		0°C-125°C, 4.5V<Vcc<5.5V	-	±6	-	%
Temperature Resolution			-	1	-	°C
Temperature Filter Rate			-	4	-	kHz
Temperature Update Rate			-	189	-	kHz
Temperature Monitoring Range			-40	-	150	°C
Temperature Reporting Accuracy			-	±1	-	°C
Thermal Shutdown			-	140	-	°C
Thermal Shutdown Hysteresis			-	20	-	°C
Input Power Resolution			-	0.5	-	W
Input Power Reporting Range			-	-	1024	W
Input Power Filter Rate			-	8	-	kHz
Input Power Update Rate			-	379	-	kHz
Input Power Accuracy			-	±3	-	%

Note:

11. *Guaranteed by design and not tested in production*

Electrical Specifications

12. *Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production.*

8 Typical Efficiency and Power Loss Curves

8.1 PV$_{in}$ = 12 V, F$_{sw}$ = Varying

The test for efficiency was done at 0 LFM and the driver losses are included in the efficiency numbers. Solid line indicate Efficiency and dashed lines are showing power loss.

Table 1   **Inductors for PV$_{in}$=12 V, F$_s$ = varying**

Vout (V)	Lout (nH)	P/N	Frequency(kHz)	DCR (mΩ)	Inductor Size (mm³)
1.1 (Ext. Vcc)	100	L101247A-100L	600	0.125	10 x 6.4 x 12
			800		
			1000		
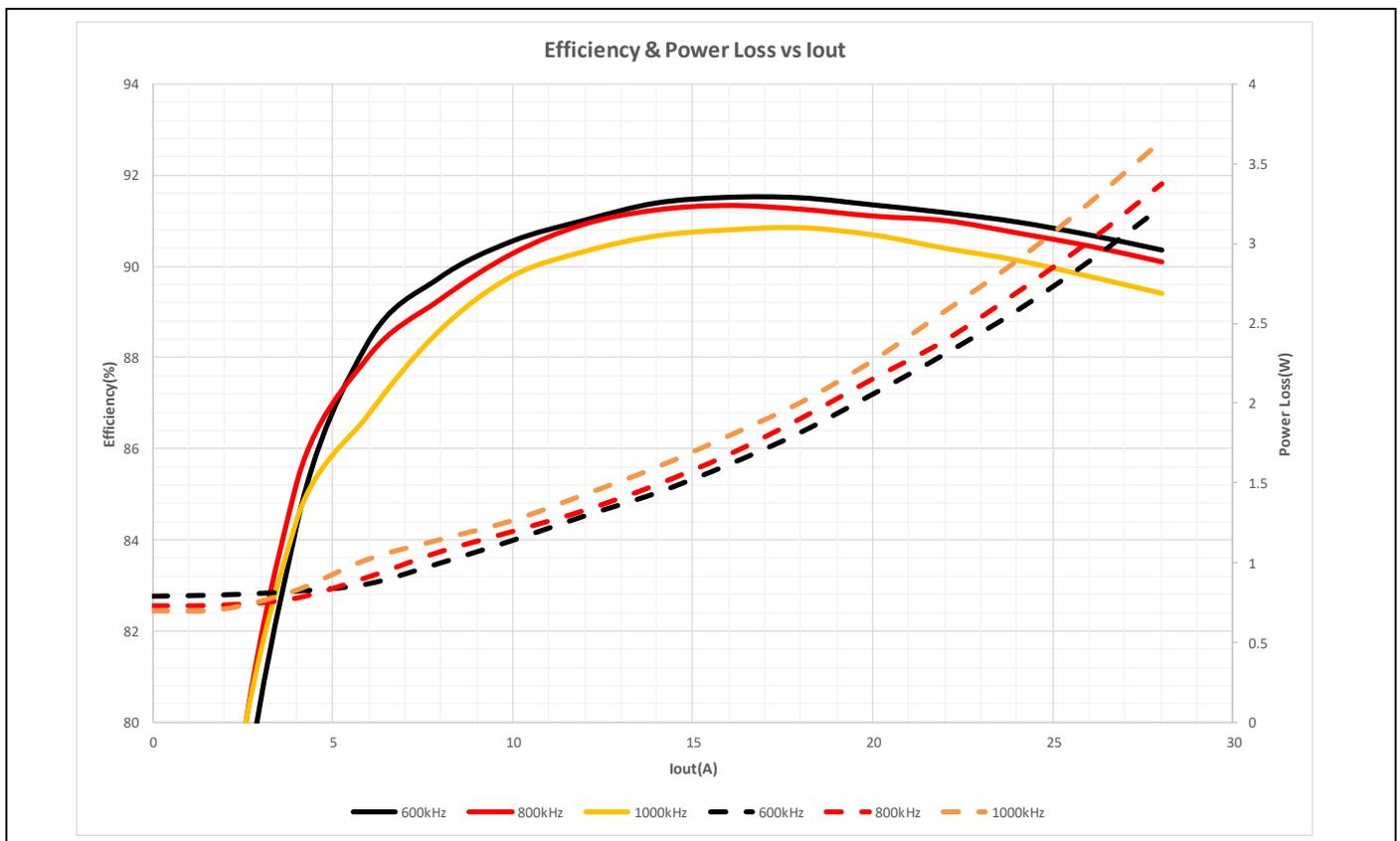
Figure 6   **Typical efficiency and power loss curves, PV$_{in}$ = 12 V, F$_{sw}$ = Varying**

Typical Efficiency and Power Loss Curves

8.2 PV$_{in}$ = 12 V, F$_{sw}$ = 800 kHz

The test for efficiency was done at 0 LFM and the driver losses are included in the efficiency numbers. Solid line indicate Efficiency and dashed lines are showing power loss.

Table 2   **Inductors for PV$_{in}$=12 V, F$_{sw}$ = 800 kHz**

Vout (V)	Lout (nH)	P/N	Frequency(kHz)	DCR (mΩ)	Inductor Size (mm³)
1.1 (Ext. Vcc)	100	L101247A-100L	800	0.125	10 x 6.4 x 12
1.1 (Int. Vcc)					
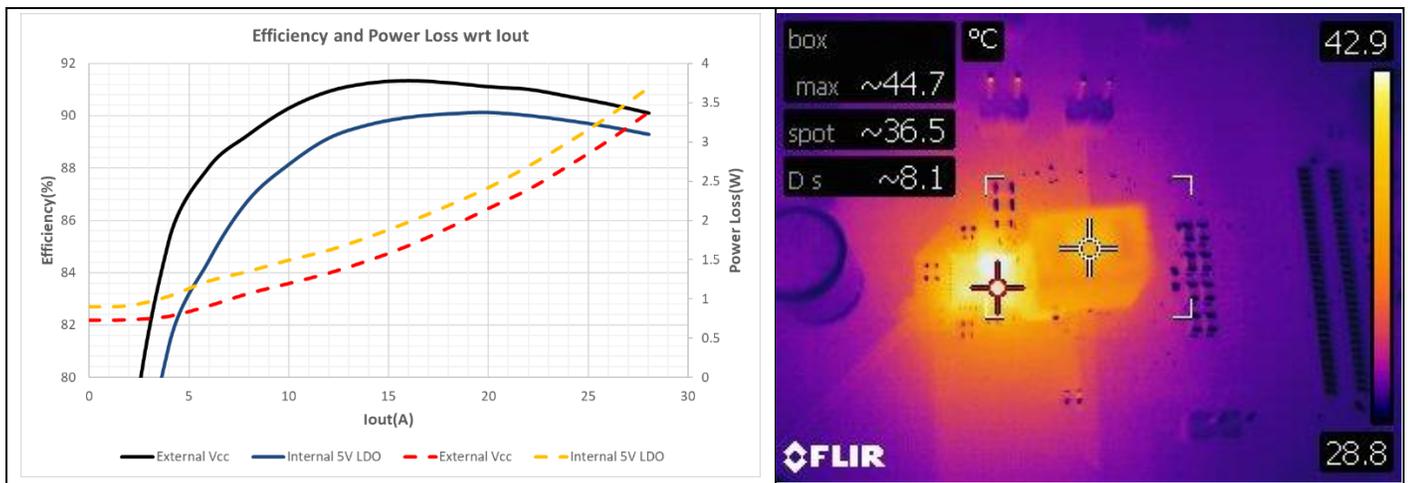
Figure 7   **Typical efficiency & power loss curve plus thermal image at full load of 28 A with Internal LDO, PV$_{in}$ = 12 V, F$_{sw}$ = 800 kHz**

8.3 PV$_{in}$ = Varying, F$_{sw}$ = 1000 kHz

The test for efficiency was done at 0 LFM and the driver losses are included in the efficiency numbers. Solid line indicate Efficiency and dashed lines are showing power loss.

Table 3   **Inductors for PV$_{in}$=Varying, F$_{sw}$ = 1000 kHz**

Vout (V)	Lout (nH)	P/N	PVIN(V)	DCR (mΩ)	Size (mm)
1.1 (Int. Vcc)	100	L101247A-100L	10.8	0.125	10 x 6.4 x 12
			12		
			13.2		

Typical Efficiency and Power Loss Curves
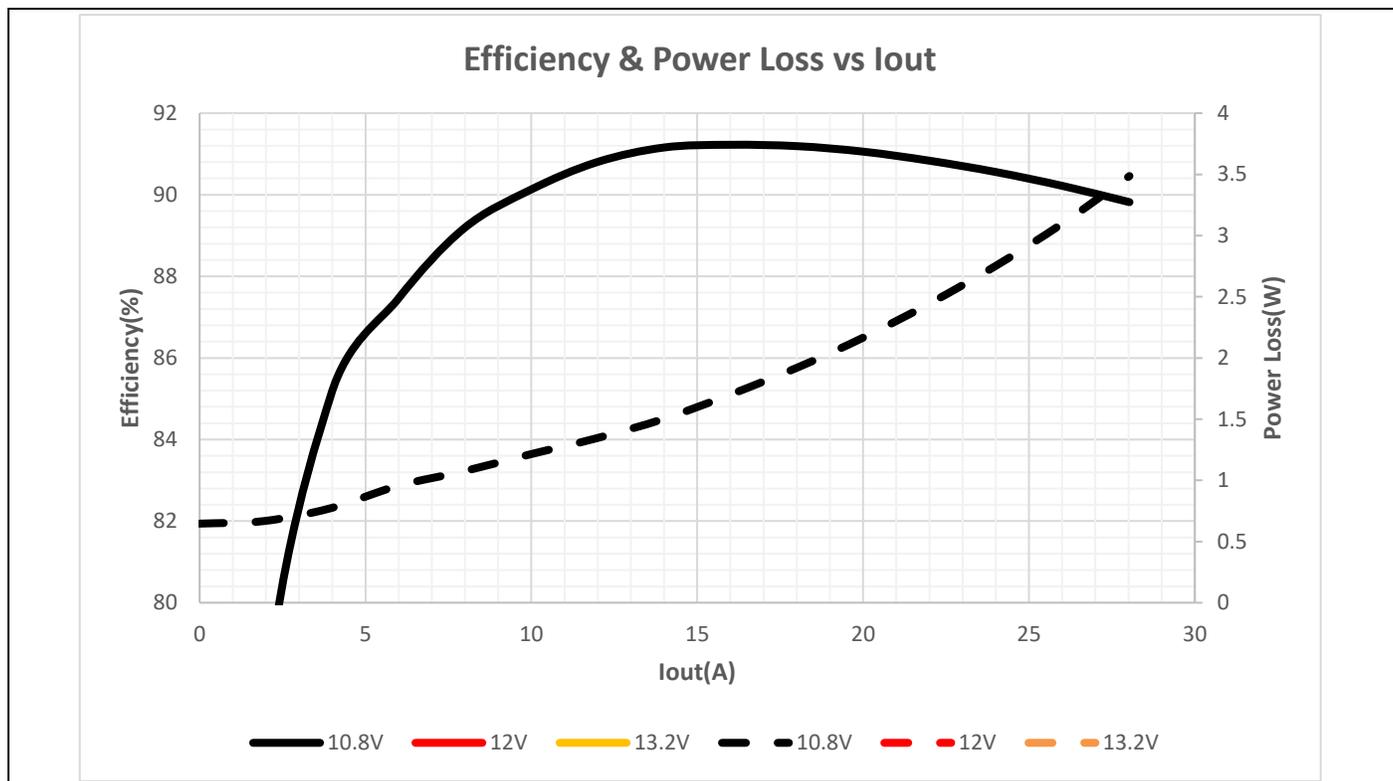
Figure 8 **Typical efficiency and power loss curves, PV$_{in}$ = Varying, F$_{sw}$ = 1000 kHz**

9 Thermal De-rating curves

This test is done on a DB356 Rev 2 Evaluation Board for TDA38640. It is an 8-layer board with 1 oz inner Cu layers and 2 oz on the top and bottom layer. FR4 material and the size of the eval board is 105 mm x 133 mm.
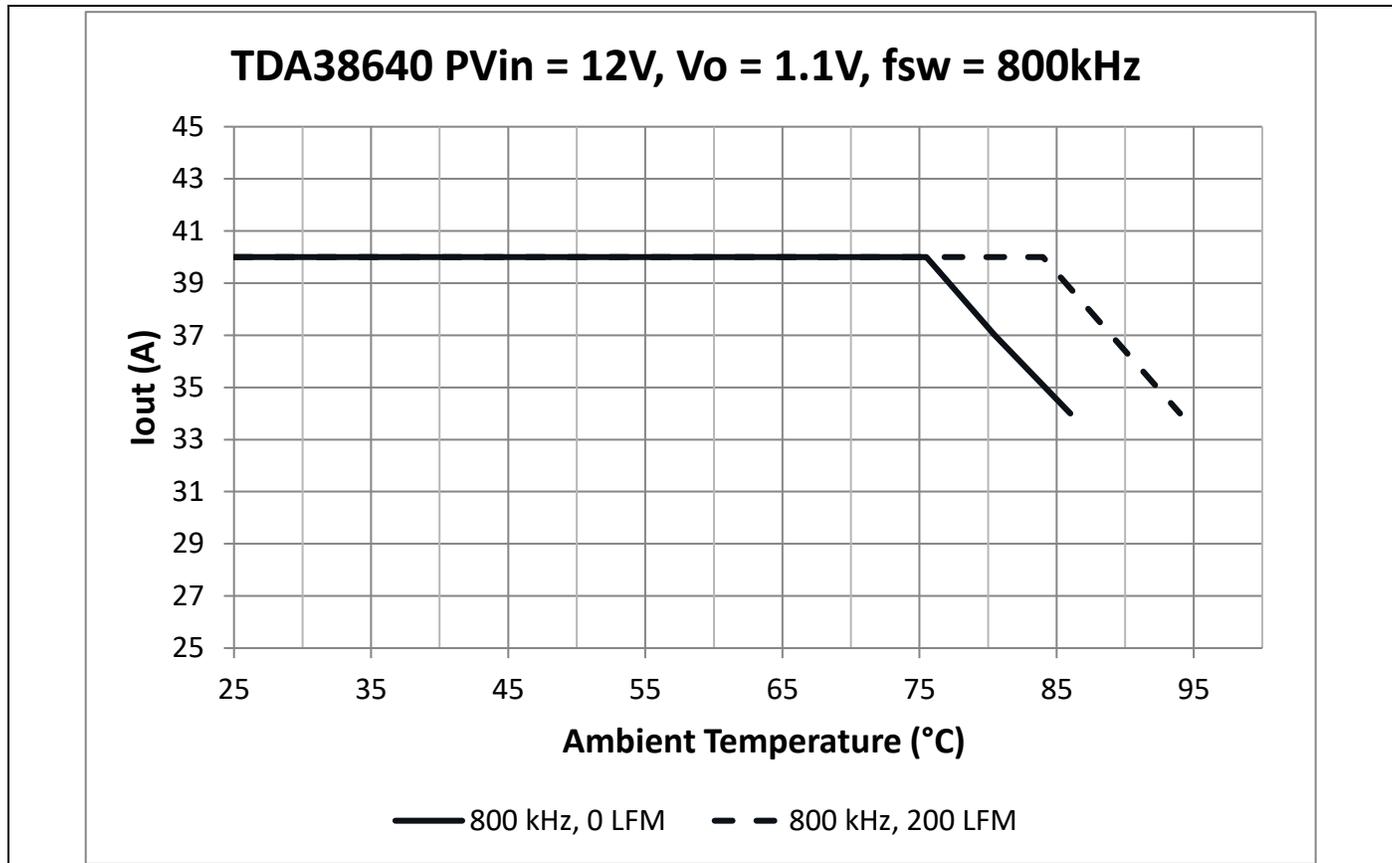
Figure 9 Thermal de-rating curves, PV_{in} = 12 V, V_{out}=1.1 V, f_{sw} = 800 kHz, VCC = Internal LDO

10 $R_{DS(ON)}$ of MOSFET Over Temperature
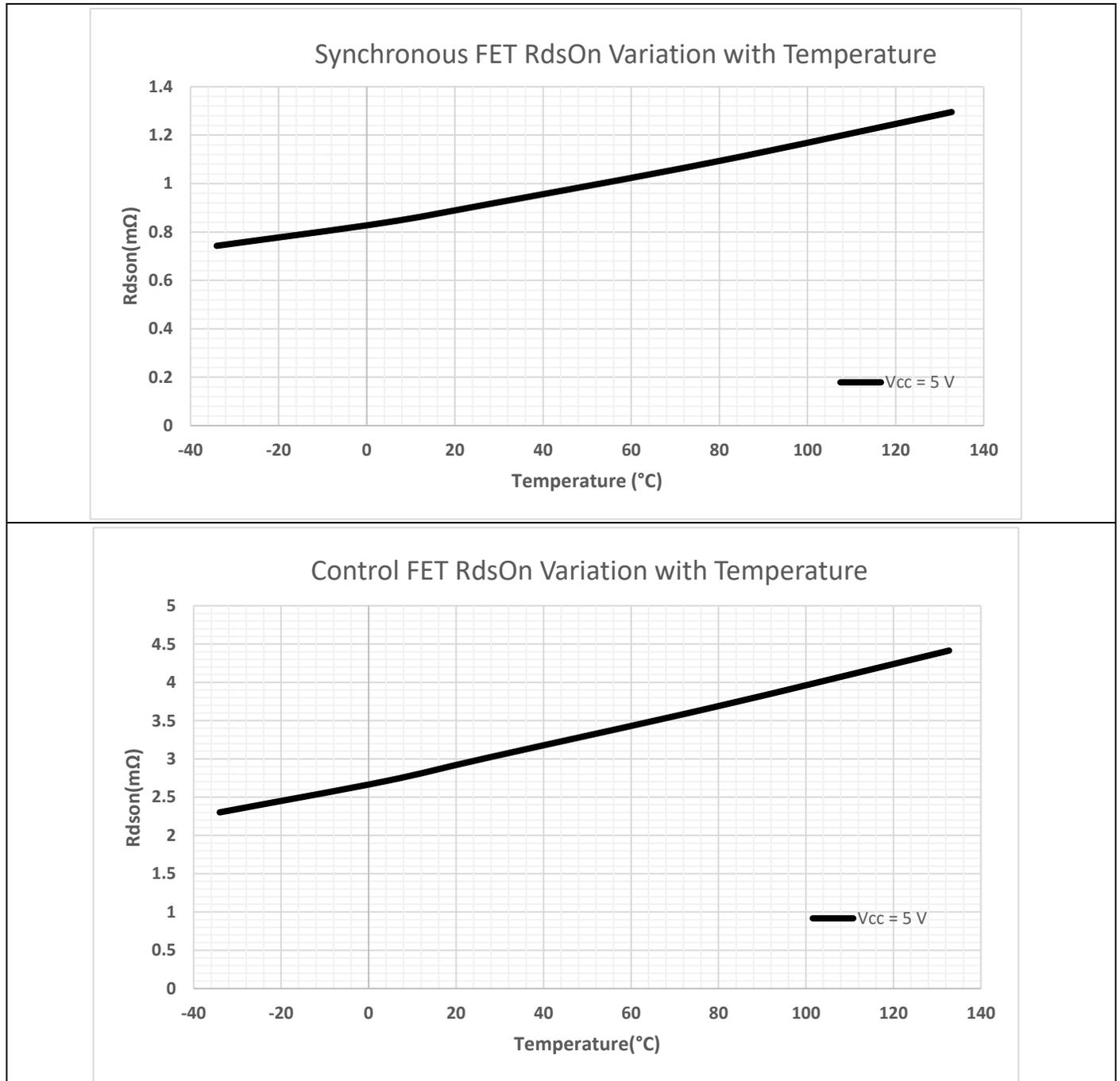
Figure 10 $R_{DS(on)}$ of MOSFETs over Junction Temperature

11 Typical operating characteristics (-40 °C ≤ T$_j$ ≤ +125 °C)
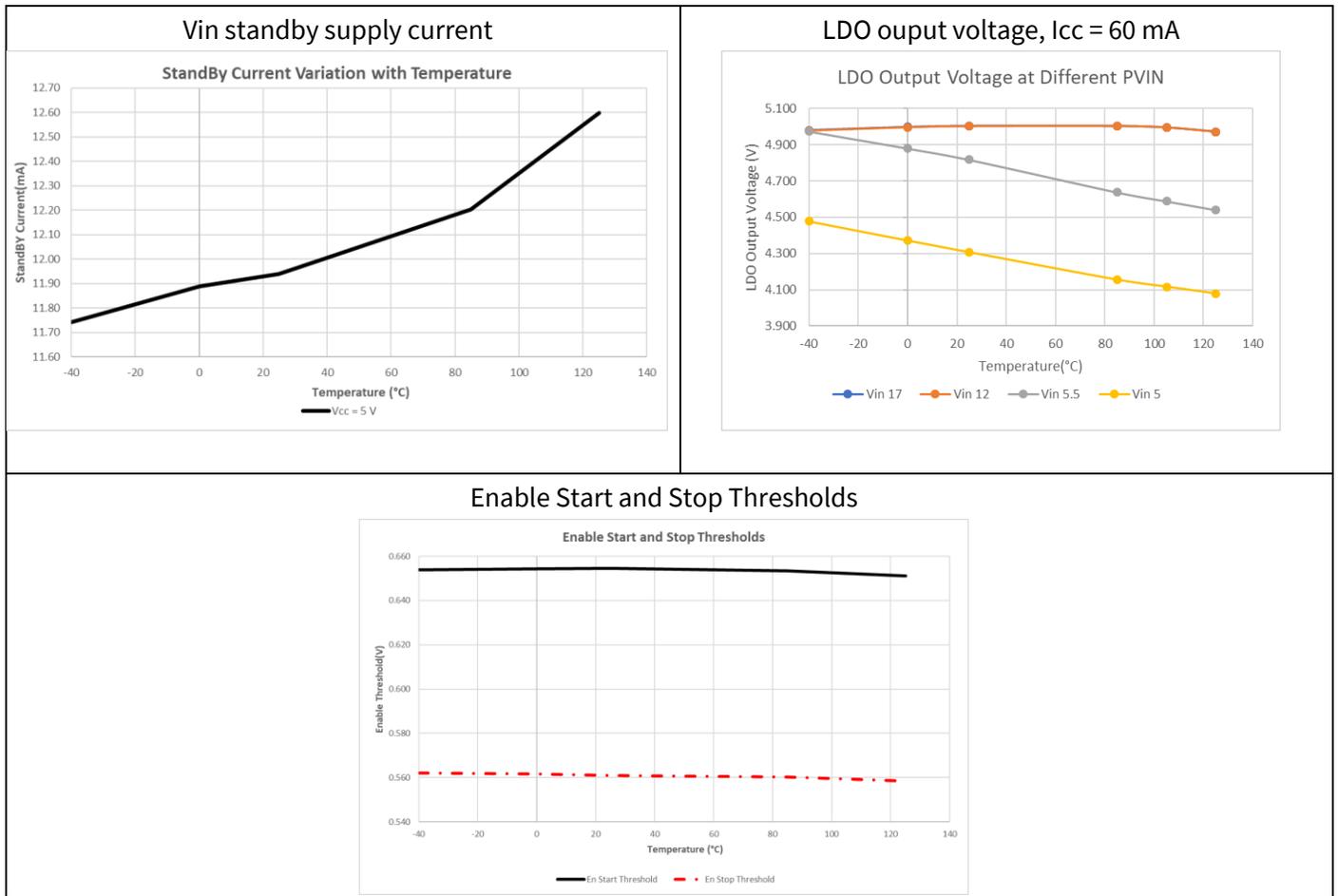
Figure 11   Typical operating characteristics (set 1 of 2)

Typical operating characteristics (-40 °C ≤ Tj ≤ +125 °C)
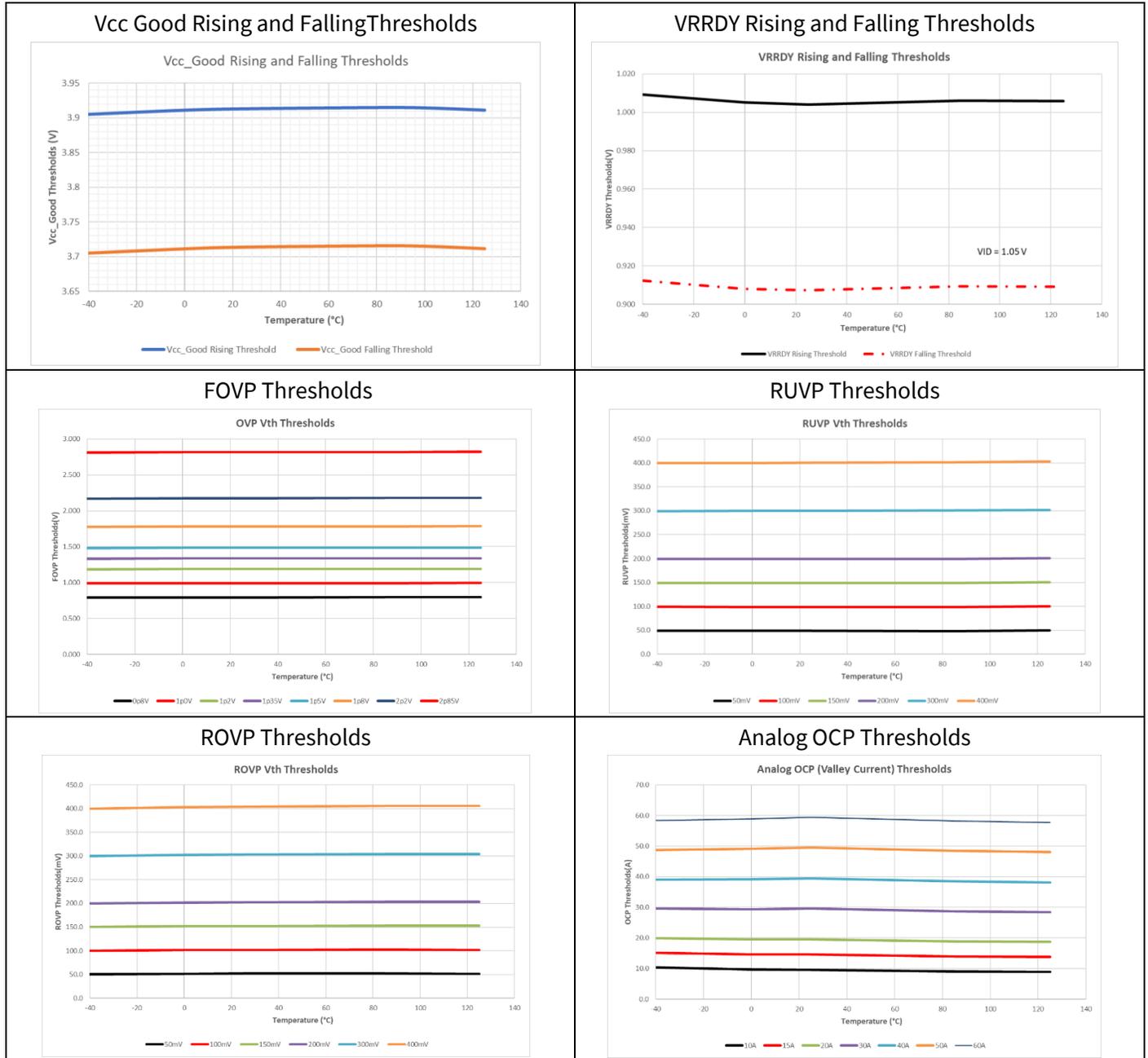
Figure 12   Typical operating characteristics (set 2 of 2)

12 General Description

The TDA38640 is an easy-to-use, fully integrated, and highly efficient DC/DC regulator optimized to convert a 12V input supply to a voltage level required by high performance microprocessors and DDR memory. The onboard PWM controller and OptiMOS™ FETs with integrated bootstrap diode make TDA38640 a small footprint solution, providing high-efficient power delivery. Using a fast Constant On-Time (COT) control scheme simplifies the design efforts and achieves fast control response. The device configuration can be easily defined using Infineon's PowerClient GUI and is stored in the on-chip memory.

12.1 Intel Operating Mode

The TDA38640 can be used for Intel® VR12, VR 12.5, VR13, VR14, IMPVP8 designs and DDR Memory without significant changes to the Bill of Materials (BOM). The required mode is selected in MTP and the pin-out, VID table and other relevant functions are automatically configured. This greatly reduces time-to-market and eliminates the need to manage and inventory different PWM controllers.

12.2 PMBUS Operating Mode

The TDA38640 can be used in PMBUS mode. The required mode is selected in MTP using GUI using the register 0x44[15]. In PMBUS mode, the output voltage is controlled by the PMBUS VOUT_COMMAND command. The VOUT_COMMAND resolution can be set to 0.244mV/lsb, 1.953mV/lsb, or 3.906mV/lsb. The output voltage resolution can only be set to a minimum of 0.625mV/lsb. The resolution is user-programmable via a configuration file.

See Table 17 for a full list of all supported PMBUS commands. Please refer to App Not Uxxxx and UNxxxx for more details.

12.3 Multiple Time Programming Memory

The multiple time programming memory (MTP) stores the device configuration. At power-up, MTP contents are transferred to operating registers for access during device operation. MTP allows customization during both design and high-volume manufacturing. MTP integrity is verified by Cyclic Redundancy Code (CRC) checking on each power up. The controller will not start up in the event of a CRC error.

The TDA38640 offers up to 48 writes to configure basic device parameters such as frequency, fault operation characteristics, and boot voltage. This represents a significant size and component saving compared to traditional analog methods. In addition to this, the TDA38640 also allows loading of multiple (up to 48) configuration files and automatic selection of a unique file after power-up based on the resistor value at the SM-ADDR/PROG pin and the pointer (0x00[13:8]).

12.4 Voltage Sense

An error voltage is generated from the difference between the target voltage, defined by the VID and load line (if implemented), and the differentially sensed output voltage (remote sense). The error voltage is digitized by a high-speed, high-precision ADC. An anti-alias filter provides the necessary high frequency noise rejection. The gain and offset of the voltage sense circuitry for each loop is factory trimmed to deliver the required accuracy.

12.5 VID Decoder

The VID decoder receives a VID code from the CPU that is converted to an internal code representing the VID voltage. The 8-bit VID code supports Intel® VR13, VR14. Also, the user can program 5mV or 10mV VID step depending on the protocol id selected by the user.

12.6 I2C & PMBus Interface

An I2C or PMBus interface is used to communicate with the TDA38640. This two-wire serial interface consists of clock and data signals, and operates as fast as 1MHz. The bus provides read & write access to the internal registers for configuration, and for monitoring of operating parameters. The bus is also used to program on-chip non-volatile memory (MTP) to store operating parameters.

To ensure operation with multiple devices on the bus, an exclusive address for the TDA38640 is programmed into MTP.

To protect customer configuration and information, the I2C interface can be configured for either limited access or locked with a 16-bit software password. Limited access includes both write and read protection options. In addition, there is a telemetry-only mode which only allows reads from the telemetry registers.

Refer to the PMBus Command Codes in Table 17 for more information. The I2C pins also allow access to the PMBus resgiters in the device.

12.7 Infineon XDP Designer GUI

The Infineon XDP Designer GUI provides the designer with a comprehensive design environment that includes input settings, output settings, telemetry, PMBus interface, and SVID settings. With these tools, a designer can monitor and set-in real-time system configuration settings for fault thresholds and output behavior. The XDP Designer GUI allows real-time design monitoring of key parameters such as output current and power, input current and power, efficiency, temperature, and faults. Figure 13 and Figure 14 show the GUI home screen and design tools with the available parameter windows. The GUI is available to download from Infineon website with in the Toolbox utility
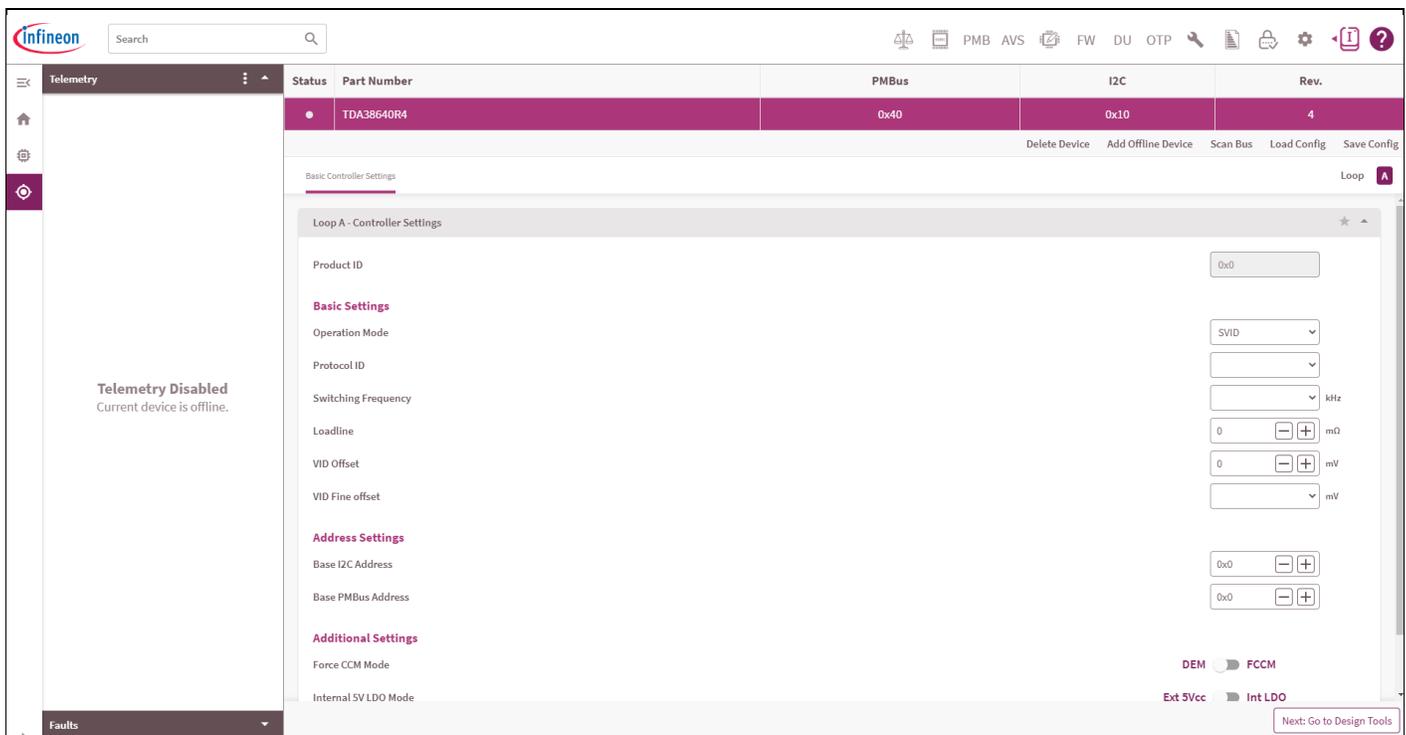
Figure 13   Snapshot of the XDP Designer GUI Homescreen for TDA38640 working in Offline Mode
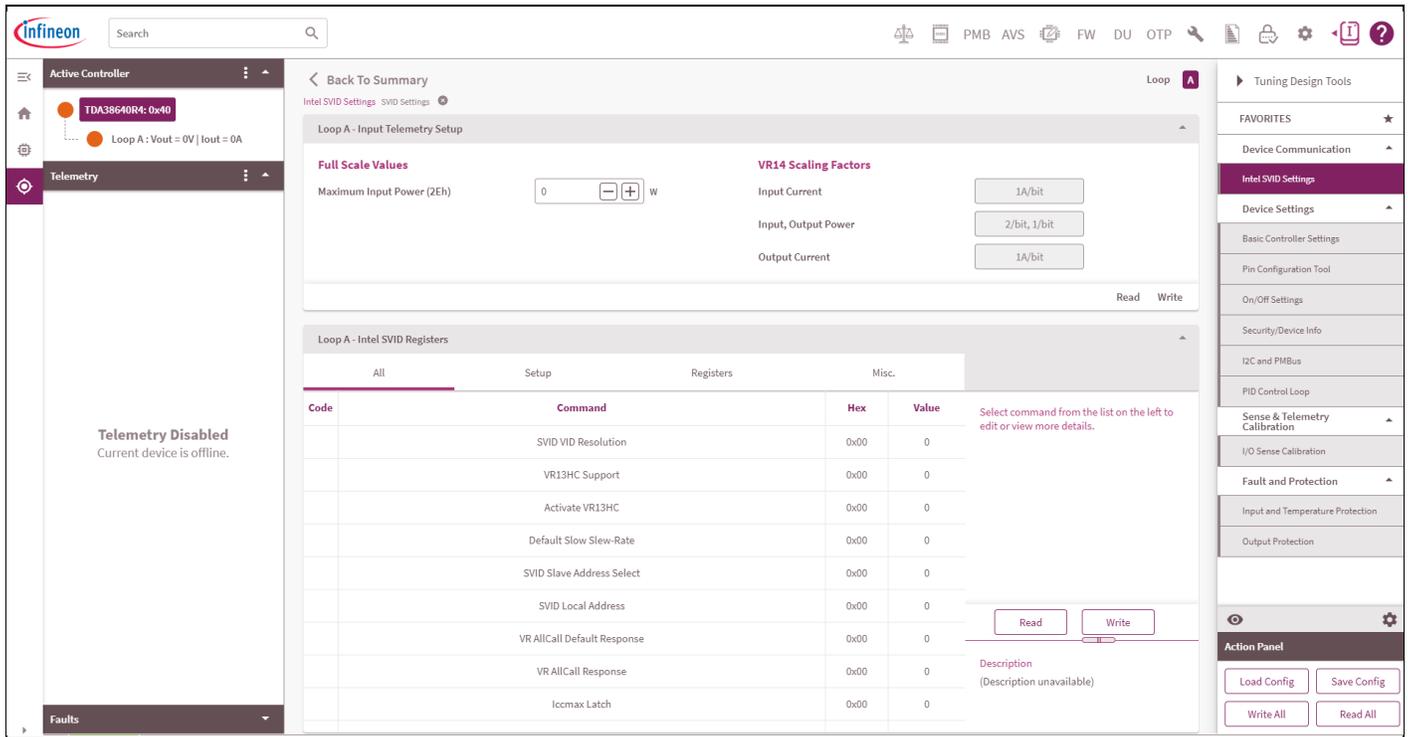
Figure 14   Snapshot of the XDP Designer GUI Design Tools for TDA38640 working in Offline Mode

12.8   Programming

Once a design is complete, the XDP Designer GUI produces a complete configuration file. These configurations files can be saved and loaded.

12.9   Real-time Monitoring

The TDA38640 can be accessed through the use of PMBus Command codes (described in Table 17), to read the real time status of the VR system including input voltage, output voltage, input and output current, input and output power and temperature.

13 Theory of Operation

13.1 Operating Mode

The TDA38640 changes its functionality based on the user-selected operating mode, allowing one device to be used for multiple applications without significant BoM changes. This greatly reduces the user's design cycles and time-to-market (TTM).

The functionality for each operating mode is completely configurable by simple selections in MTP. The mode configuration is shown in Table 7. The mode can be selected based on the i2c register 0x44[12:8], this is the protocol-id register which selects the Intel Mode for which the device is being used.

Table 7   Mode Selection

Mode	Description
VR14	Intel® VR14 (Selected via MTP).
VR13	Intel® VR13 (Selected via MTP).
VR12.X	Intel® VR12.X (Selected via MTP).

13.2 Device Power-On

TDA38640-xxxx is ready to communicate as soon as Vcc is above the the threshold of 3.6 V. The device starts switching once the Enable signal is pulled high. Based on whether Vcc is supplied externally or an internal LDO is used the recommended power-up sequences are shown in Figure 15.
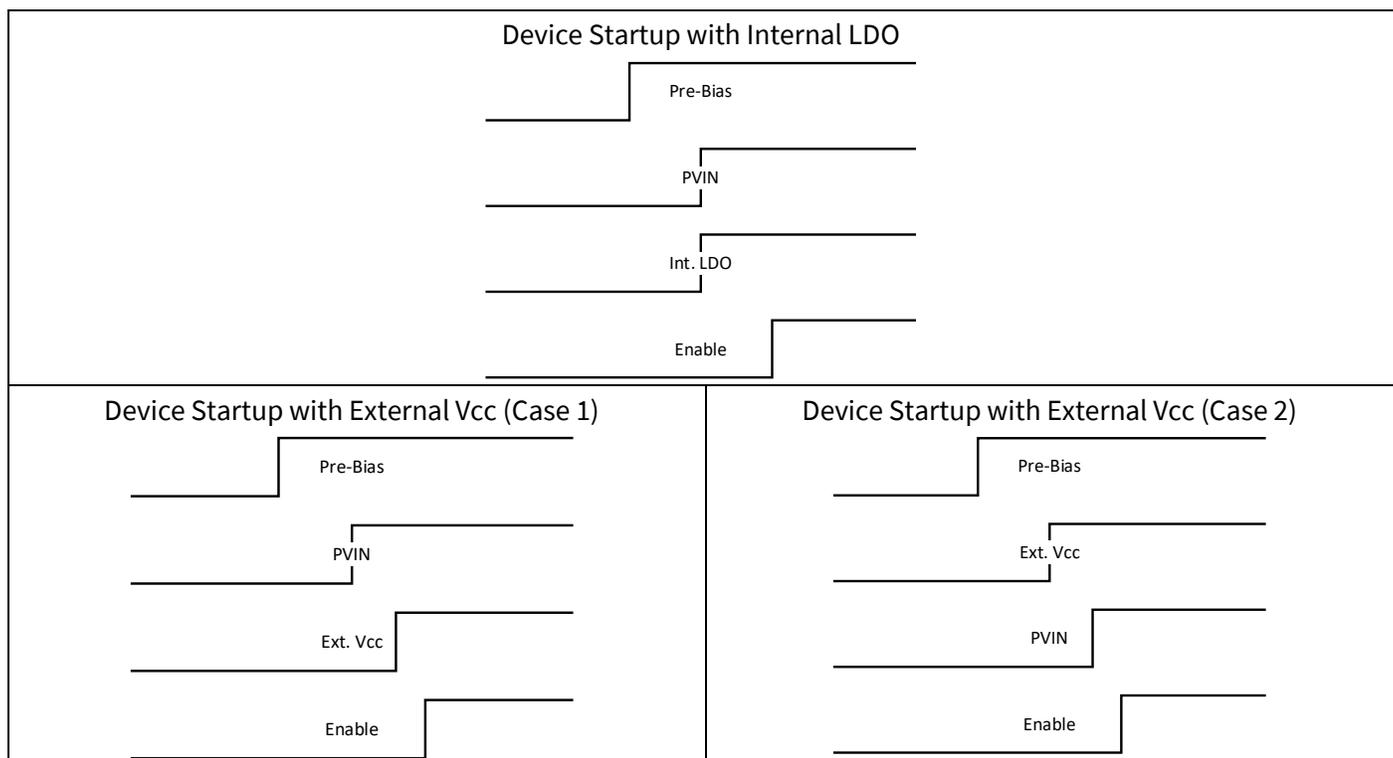
Figure 15   Device power-on sequence with pre-bias.

13.3 Pre-bias start-up

The TDA38640 is able to start up into a pre-charged output without causing oscillations and disturbances of the output voltage. When TDA38640 starts up with a pre-biased output voltage, both control FET and Synch FET are kept off until the internal soft-start signal exceeds the FB voltage. The sequencing recommendation with pre-bias is shown in Figure 15.

13.4 Internal Low-Dropout (LDO) Regulator

The TDA38640 has an integrated low-dropout LDO regulator, providing the bias voltage for the internal circuitry. To minimize the standby current, the internal LDO is disabled when the En voltage is pulled low. VIN pin is the input of the LDO. When using the internal LDO for a single rail operation, VIN pin should be connected to PVIN pin. To save the power losses on the LDO, an external bias voltage can be used by connecting VIN pin to the VCC/LDO pin. Figure 16 illustrates the possible configurations of VCC/LDO, and VIN pin.
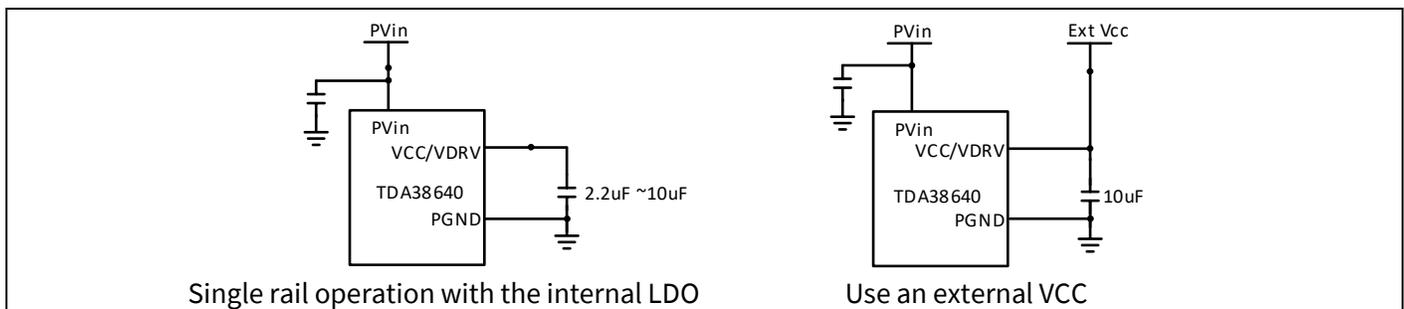
Figure 16   Configuration of using the internal LDO or an external VCC.

13.5 Fast Constant ON-Time Control

The TDA38640 features a proprietary Fast Constant On-Time (COT) Control, which can provide fast load transient response, good output regulation and minimize the design effort. Fast COT control compares the output voltage, V_o, to a floor voltage combined with an internal ramp signal. When V_{out} drops below that signal, a PWM signal is initiated to turn on the high-side FET for a fixed on-time. The floor voltage is generated from an internal compensated error amplifier, which compares the Vout with a reference voltage. Compared to the traditional COT control, Fast COT control significantly improves the Vout regulation.

13.6 Enable

Enable pin controls the on/off of the TDA38640. When the En voltage is above an internal threshold, the internal LDO starts to ramp up. When the VCC/LDO voltage rises above the VCC_UVLO_Start threshold, the soft-start sequence starts.

The EN pin can be configured in three ways. Two of them are as shown in Figure 17. Configuration one is an external logic signal. The second possible configuration derives the enable signal from the PVin voltage by a resistive divider, R_{EN1} and R_{EN2}. The third configuration is control via PMBus register 0x204[7:0] using the PMBus lines. TDA38640 utilizes the PMBus ON_OFF_CONFIG command in combination with OPERATION command, register 0x202[7:0], to control the soft enable. Using this a preference between hardware or software enable may be established. More information is available in the PMBUs app note UNxxxx.

Theory of Operation

Note that the absolute maximum En to PGND voltage for the TDA38640 is 6V, so a divider must be used with enable tied to the input. The EN pin should not be left floating. A pull-down resistor in the range of tens of kilohms is recommended.

$$En = \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \times PV_{in}$$

En = an external logic signal

Configuration 1   Configuration 2
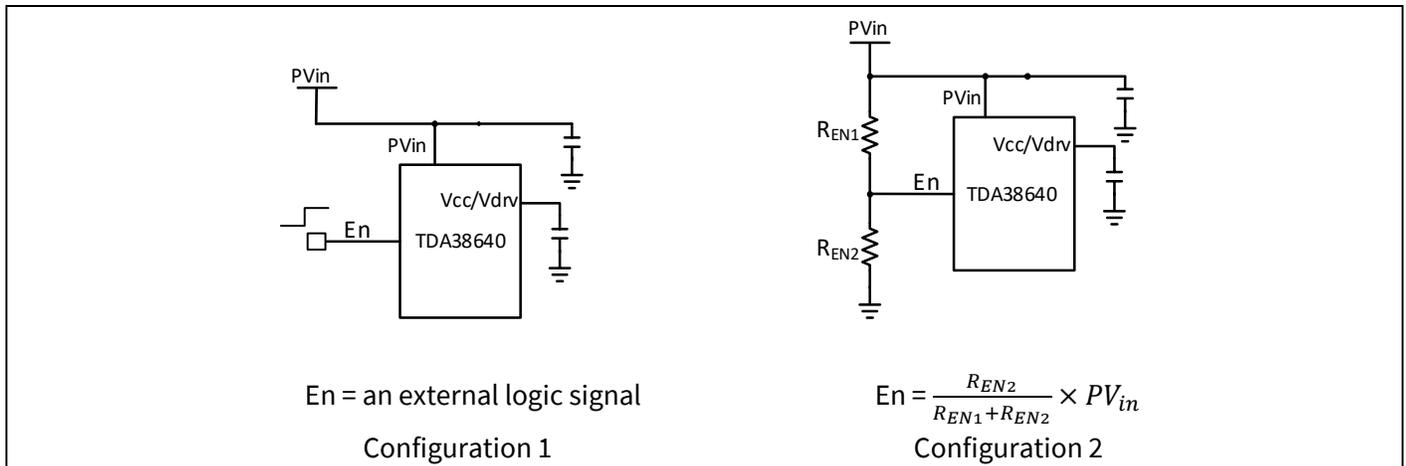
Figure 17 Enable Configurations

13.7 Switching Frequency and FCCM/DEM Operation

TDA38640 offers two operation modes: Forced Continuous Conduction (FCCM) and Diode Emulation Mode (DEM). With FCCM, the TDA38640 always operates as a synchronous buck converter with a pseudo constant switching frequency and therefore achieves small output voltage ripples. In DEM, the synchronous FET is turned off when the inductor current is close to zero, which reduces the switching frequency and improves the efficiency at light load. At heavy load, both FCCM and DEM operate in the same way. The operation mode can be selected by bit 0x5A [1], value 1 for this bit programs the device to operate in FCCM mode and 0 for DEM. It should be noted that the selection of the operation mode cannot be changed on the fly. To load a new configuration, En or VCC voltage needs to be cycled.

The TDA38640 offers eight programmable switching frequencies, f_{sw}, from 400 kHz to 2 MHz excluding 1600 kHz, by editing the PMBus register, 0x266[16:0], using the I2C lines. Based on the selected f_{sw}, the TDA38640 generates the corresponding on-time of the Control FET for a given PV_{in} and V_o, as shown by the formula below.

$$T_{on} = \frac{V_0}{PV_{in}} \times \frac{1}{f_{sw}}$$

Where f_{sw} is the desired switching frequency. During the operation, the TDA38640 monitors PV_{in} and V_o, and can automatically adjust the on-time to maintain the pre-selected f_{sw}. With the increase of the load, the switching frequency can increase to compensate for the power losses. Therefore, the TDA38640 has a pseudo constant switching frequency.

To load a new TON/MODE configuration, En or VCC voltage needs to be cycled.

Using the FREQUENCY_SWITCH PMBus command, the switching frequency may be programmed between 400 kHz and 2 MHz in steps of 200Hz except 1600Hz.

13.8 Intel Mode

When the power-on sequence is initiated, and with VBOOT set to > 0V, the output voltage will ramp to its configured boot voltage and assert VRRDY. The slew rate to VBOOT is programmed per VID_FAST/VID_SLOW commands.

If Vboot = 0V, the VR will stay at 0V and will not soft-start until the CPU issues a VID command to the loop. In VR13 mode, as soon as the IC is ready for SVID communication, SV_ALERT# will be asserted with Vboot = 0V.

13.8.1 Intel Boot Mode

The TDA38640 Vboot voltage is fully programmable in MTP to the range specified in the Intel VID tables. Table 8 and Table 9 show the Intel VID tables for 5mV and 10mV VID steps respectively.

13.8.2 Intel SVID Interface

The TDA38640 implements a fully compliant Intel® VR 13, VR12, VR 12.5, and VR14 Serial VID (SVID) interface. This is a 3-wire interface between an Intel processor & VR that consists of clock, data and alert# signals.

The TDA38640 implements all the required SVID registers and commands per Intel specifications. For the selected Intel mode, the TDA38640 also implements most of the optional commands and registers with very few exceptions. The Intel CPU is able to detect and recognize the extra functionality that the TDA38640 provides and thus gives the Intel® VR 14/13/12/12.5 CPU unparalleled ability to monitor and optimize its power.

The SVID address of the TDA38640 defaults to 0. This address can be re-programmed in MTP. An address lock function prevents accidental overwrites of the address.

The pseudo-code below illustrates the MTP address programming:

```
# unlock the address register to write, then lock
Set Address_lock_bit=0
Write new SVID address
```

13.8.3 All Call SUPPORT

All Call for each loop of TDA38640 can be configured in following ways:

- 0E and 0F.
- 0E only.
- 0F only.
- No All Call

TDA38640 can be configured to be used as VR for CPU which is All Call 0F or Memory which is All Call 0E.

13.8.4 VR13 Operation

VR 13 mode is selectable via MTP bit (0x44[12:8]). The boot voltage in VR 13 mode is configured in the boot register. In VR 13 mode, the boot voltage can be configured in 5mV steps or 10mV steps.

13.8.5 VR14 Operation

VR 14 mode is selectable via MTP bit (0x44[12:8]). The boot voltage in VR 14 mode is configured in the boot register. In VR 14 mode, the boot voltage can be configured in 5mV steps) or 10mV steps.

13.8.6 Set Work Point

TDA38640 supports SVID Set WP command to Set VID voltage for all rails through all call address. When processor asserts a Set WP command, all the rails of the VR settle to the corresponding new set-voltage encoded in WP registers. Slew rate and power state of all the rails are identical during a set work point operation.

Table 8   Intel 5mV VID Table (VR14 and VR13)

VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)
FF	1.52	DA	1.335	B5	1.15	90	0.965	6B	0.78
FE	1.515	D9	1.33	B4	1.145	8F	0.96	6A	0.775
FD	1.51	D8	1.325	B3	1.14	8E	0.955	69	0.77
FC	1.505	D7	1.32	B2	1.135	8D	0.95	68	0.765
FB	1.5	D6	1.315	B1	1.13	8C	0.945	67	0.76
FA	1.495	D5	1.31	B0	1.125	8B	0.94	66	0.755
F9	1.49	D4	1.305	AF	1.12	8A	0.935	65	0.75
F8	1.485	D3	1.3	AE	1.115	89	0.93	64	0.745
F7	1.48	D2	1.295	AD	1.11	88	0.925	63	0.74
F6	1.475	D1	1.29	AC	1.105	87	0.92	62	0.735
F5	1.47	D0	1.285	AB	1.1	86	0.915	61	0.73
F4	1.465	CF	1.28	AA	1.095	85	0.91	60	0.725
F3	1.46	CE	1.275	A9	1.09	84	0.905	5F	0.72
F2	1.455	CD	1.27	A8	1.085	83	0.9	5E	0.715
F1	1.45	CC	1.265	A7	1.08	82	0.895	5D	0.71
F0	1.445	CB	1.26	A6	1.075	81	0.89	5C	0.705
EF	1.44	CA	1.255	A5	1.07	80	0.885	5B	0.7
EE	1.435	C9	1.25	A4	1.065	7F	0.88	5A	0.695
ED	1.43	C8	1.245	A3	1.06	7E	0.875	59	0.69
EC	1.425	C7	1.24	A2	1.055	7D	0.87	58	0.685
EB	1.42	C6	1.235	A1	1.05	7C	0.865	57	0.68
EA	1.415	C5	1.23	A0	1.045	7B	0.86	56	0.675
E9	1.41	C4	1.225	9F	1.04	7A	0.855	55	0.67
E8	1.405	C3	1.22	9E	1.035	79	0.85	54	0.665
E7	1.4	C2	1.215	9D	1.03	78	0.845	53	0.66
E6	1.395	C1	1.21	9C	1.025	77	0.84	52	0.655
E5	1.39	C0	1.205	9B	1.02	76	0.835	51	0.65

Theory of Operation

VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)
E4	1.385	BF	1.2	9A	1.015	75	0.83	50	0.645
E3	1.38	BE	1.195	99	1.01	74	0.825	4F	0.64
E2	1.375	BD	1.19	98	1.005	73	0.82	4E	0.635
E1	1.37	BC	1.185	97	1	72	0.815	4D	0.63
E0	1.365	BB	1.18	96	0.995	71	0.81	4C	0.625
DF	1.36	BA	1.175	95	0.99	70	0.805	4B	0.62
DE	1.355	B9	1.17	94	0.985	6F	0.8	4A	0.615
DD	1.35	B8	1.165	93	0.98	6E	0.795	49	0.61
DC	1.345	B7	1.16	92	0.975	6D	0.79	48	0.605
DB	1.34	B6	1.155	91	0.97	6C	0.785	47	0.6
46	0.595	37	0.52	28	0.445	19	0.37	0A	0.295
45	0.59	36	0.515	27	0.44	18	0.365	09	0.29
44	0.585	35	0.51	26	0.435	17	0.36	08	0.285
43	0.58	34	0.505	25	0.43	16	0.355	07	0.28
42	0.575	33	0.5	24	0.425	15	0.35	06	0.275
41	0.57	32	0.495	23	0.42	14	0.345	05	0.27
40	0.565	31	0.49	22	0.415	13	0.34	04	0.265
3F	0.56	30	0.485	21	0.41	12	0.335	03	0.26
3E	0.555	2F	0.48	20	0.405	11	0.33	02	0.255
3D	0.55	2E	0.475	1F	0.4	10	0.325	01	0.25
3C	0.545	2D	0.47	1E	0.395	0F	0.32	00	0
3B	0.54	2C	0.465	1D	0.39	0E	0.315		
3A	0.535	2B	0.46	1C	0.385	0D	0.31		
39	0.53	2A	0.455	1B	0.38	0C	0.305		
38	0.525	29	0.45	1A	0.375	0B	0.3		

Table 9   Intel 10mV VID Table (VR14 and VR13)

VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)
FF	3.04	DC	2.69	B9	2.34	96	1.99	73	1.64
FE	3.03	DB	2.68	B8	2.33	95	1.98	72	1.63
FD	3.02	DA	2.67	B7	2.32	94	1.97	71	1.62
FC	3.01	D9	2.66	B6	2.31	93	1.96	70	1.61
FB	3.00	D8	2.65	B5	2.30	92	1.95	6F	1.60
FA	2.99	D7	2.64	B4	2.29	91	1.94	6E	1.59
F9	2.98	D6	2.63	B3	2.28	90	1.93	6D	1.58

Theory of Operation

VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)
F8	2.97	D5	2.62	B2	2.27	8F	1.92	6C	1.57
F7	2.96	D4	2.61	B1	2.26	8E	1.91	6B	1.56
F6	2.95	D3	2.60	B0	2.25	8D	1.90	6A	1.55
F5	2.94	D2	2.59	AF	2.24	8C	1.89	69	1.54
F4	2.93	D1	2.58	AE	2.23	8B	1.88	68	1.53
F3	2.92	D0	2.57	AD	2.22	8A	1.87	67	1.52
F2	2.91	CF	2.56	AC	2.21	89	1.86	66	1.51
F1	2.90	CE	2.55	AB	2.20	88	1.85	65	1.50
F0	2.89	CD	2.54	AA	2.19	87	1.84	64	1.49
EF	2.88	CC	2.53	A9	2.18	86	1.83	63	1.48
EE	2.87	CB	2.52	A8	2.17	85	1.82	62	1.47
ED	2.86	CA	2.51	A7	2.16	84	1.81	61	1.46
EC	2.85	C9	2.50	A6	2.15	83	1.80	60	1.45
EB	2.84	C8	2.49	A5	2.14	82	1.79	5F	1.44
EA	2.83	C7	2.48	A4	2.13	81	1.78	5E	1.43
E9	2.82	C6	2.47	A3	2.12	80	1.77	5D	1.42
E8	2.81	C5	2.46	A2	2.11	7F	1.76	5C	1.41
E7	2.80	C4	2.45	A1	2.10	7E	1.75	5B	1.40
E6	2.79	C3	2.44	A0	2.09	7D	1.74	5A	1.39
E5	2.78	C2	2.43	9F	2.08	7C	1.73	59	1.38
E4	2.77	C1	2.42	9E	2.07	7B	1.72	58	1.37
E3	2.76	C0	2.41	9D	2.06	7A	1.71	57	1.36
E2	2.75	BF	2.40	9C	2.05	79	1.70	56	1.35
E1	2.74	BE	2.39	9B	2.04	78	1.69	55	1.34
E0	2.73	BD	2.38	9A	2.03	77	1.68	54	1.33
DF	2.72	BC	2.37	99	2.02	76	1.67	53	1.32
DE	2.71	BB	2.36	98	2.01	75	1.66	52	1.31
DD	2.70	BA	2.35	97	2.00	74	1.65	51	1.30
50	1.29	3E	1.11	2C	0.93	1A	0.75	08	0.57
4F	1.28	3D	1.10	2B	0.92	19	0.74	07	0.56
4E	1.27	3C	1.09	2A	0.91	18	0.73	06	0.55
4D	1.26	3B	1.08	29	0.90	17	0.72	05	0.54
4C	1.25	3A	1.07	28	0.89	16	0.71	04	0.53
4B	1.24	39	1.06	27	0.88	15	0.70	03	0.52
4A	1.23	38	1.05	26	0.87	14	0.69	02	0.51
49	1.22	37	1.04	25	0.86	13	0.68	01	0.50

VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)	VID (Hex)	Voltage (V)
48	1.21	36	1.03	24	0.85	12	0.67	00	0
47	1.20	35	1.02	23	0.84	11	0.66		
46	1.19	34	1.01	22	0.83	10	0.65		

13.9 Program Pin (SM_ADDR/PROG)

A resistor to ground on this pin sets both a fixed I2C slave address offset and configuration from the multi-configuration file that will be loaded into the OTP during power-up.

Table 10   SM_ADDR/PROG Pin

Resistor to GND (kΩ)	PROG pin	SM_ADDR offset pin
SHORT	CONFIG0	0
5.62	CONFIG1	1
9.53	CONFIG2	2
14	CONFIG3	3
21	CONFIG4	4
30.1	CONFIG5	5
36.5	CONFIG6	6
43.2	CONFIG7	7
51.1	CONFIG8	8
61.9	CONFIG9	9
75	CONFIG10	10
88.7	CONFIG11	11
105	CONFIG12	12
127	CONFIG13	13
150	CONFIG14	14
FLOAT	CONFIG15	15

13.10 Soft Start

The soft-start functionality is defined to support SVID commands for soft-start SetVID_Slow (0x44[1:0]) and SetVID_Fast (0x46[15:12]) commands are used to set the soft start timing to VID.

13.11 Load-line

TDA38640 offers digital load line which can be set via configuration registers, without any need for external components. The load line can be programmed from 0 to 10 mΩ at a resolution of 19.53 µΩ using the VOUT_DROOP command 0x250[15:0]. The range and resolution of the VOUT_DROOP may be increased by using the bit

loadline_range_sel 0x6a [6] to 0 to 50 mΩ at a resolution of 100 µΩ. In addition to this, the bandwidth of the digital load line is also programmable from 30 kHz to 500 kHz in steps of 30 kHz by using 4 bits of register 0x6a [3:0].

13.12 Output Voltage Differential Sensing

The TDA38640 VSEN and VRTN pins are connected across the output capacitors near the load to provide true differential remote voltage sensing with high common-mode rejection. Fast COT control compares the output voltage to a floor voltage combined with an internal ramp signal. When Vout drops below that signal, a PWM signal is initiated to turn on the high-side FET for a fixed on-time. The floor voltage is generated from an internal compensated error amplifier, which compares the Vout with a reference voltage. As shown in Figure 18, the output sense pins VOSENP and VOSENM are connected across the output capacitors.
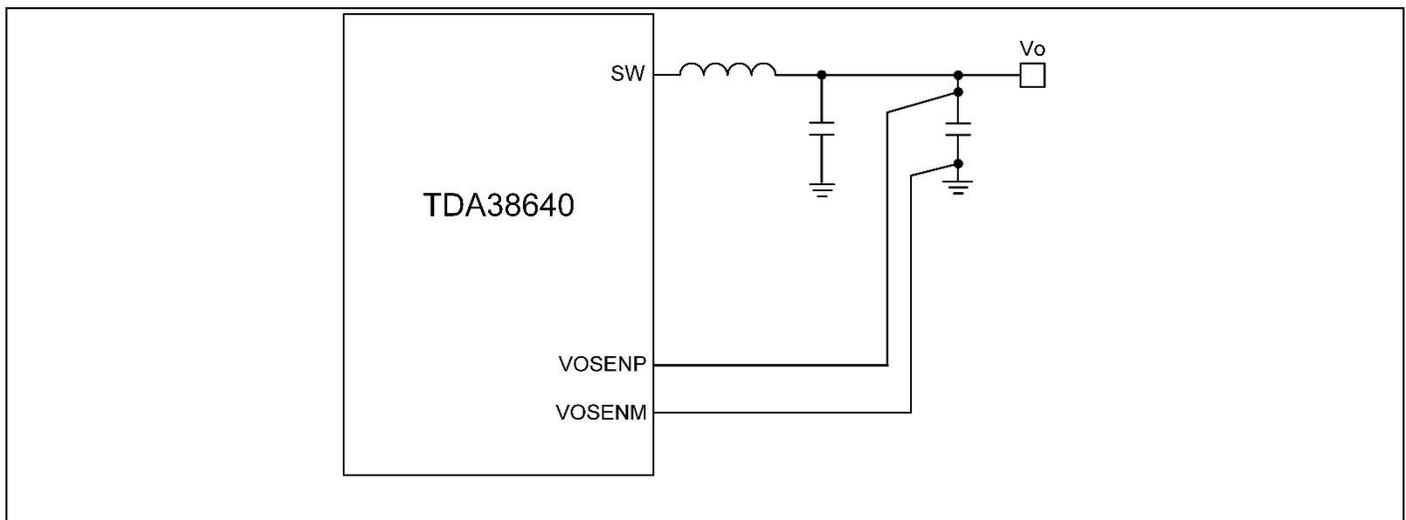
Figure 18   Output voltage sensing connections

13.13 Input Current Sensing

The TDA38640 can measure input current using a measured value from a shunt resistor and/or calculate it using other known variables. The input current sense mode is controlled by the register iin_sense_mode, with options outlined in Table 11.

Table 11   Register iin_sense_mode options.

Value	Mode
3, 2	Calculated and external resistor sense
1	External resistor sense
0	Calculated

The "lossless input current estimation" scheme can accurately calculate the actual input current as it knows the value of output current, output voltage, input voltage and pulse width of each phase. This eliminates the need for a dedicated shunt & the IINSEN pin and also simplifies the board layout by eliminating additional components.

Register iin_rsense_value control the external resistor value used for sensing. There is also offset and gain correction that is provided to the user via the iin_offset_user (0x66[13:8]) and iin_gain_user (0x66[7:4]) registers respectively.

Table 12 summarizes the usable external resistor values from iin_rsense_value (0x66[3:0]).

Figure 19 shows the generic application circuit for input current sensing in a typical application.

Table 12   Usable external input current sense resistors, from register iin_rsense_value.

Value	Threshold	Value	Threshold
11-15	10 mΩ	5	4 mΩ
10	9 mΩ	4	3 mΩ
9	8 mΩ	3	2 mΩ
8	7 mΩ	2	1 mΩ
7	6 mΩ	1	0.5 mΩ
6	5 mΩ	0	0.2 mΩ
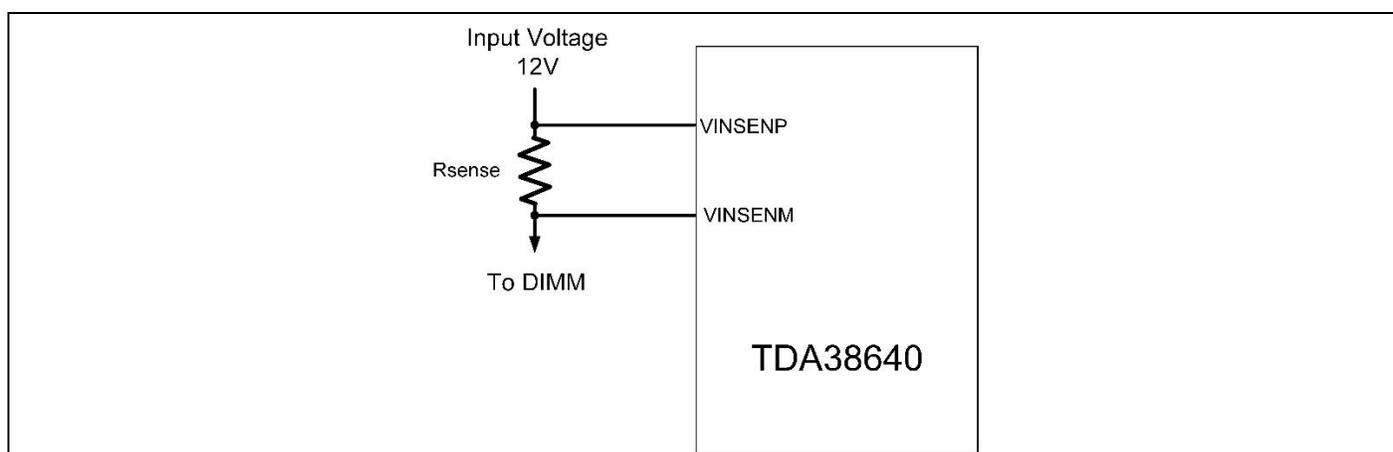
Figure 19   Input current sensing using external shunt

13.14   CAT_FAULT# and VRRDY

TDA38640 supports the CAT_FAULT functionality. This is an additional indication of a fault in the system which the system can use to take an action. The CAT_FAULT is open drain output and is pulled high to 3.3 V in the system. In case of a fault this active low signal is asserted, the conditions under the assertion is done is shown below in Table 13. The functionality is further defined in the VR14 PWM document. CAT_FAULT# is asserted to High side short during start-up, other than this the CAT_FAULT signal is nto asserted for any other fault during start-up. The signal is reset when ENABLE or VCC is recycled.

VRRDY is Intel's equivalent of PGOOD. The electrical characteristics for the signal is defined in detail in the Intel VR14 PWM document. It is an open drain output pulled up to 3.3 V. When the power-on sequence is initiated, and with VBOOT set to > 0V, the output voltage will ramp to its configured boot voltage and assert VRRDY.

Table 13   VRRDY and CAT_FAULT# Response to Faults

Type of Fault	VRRDY Pin Functionality	CATFLT Pin Functionality	Device Behaviour after event
OVP	This pin is deasserted	This pin is asserted	Latched Shutdown
OCP	This pin is deasserted	This pin is asserted	Latched Shutdown
UVP	This pin is deasserted	This pin is asserted	Latched Shutdown
Boot UVLO	This pin is deasserted	This pin is asserted	Latched Shutdown
Vcc UVLO	This pin is deasserted	This pin is asserted	Latched Shutdown
OTP	This pin is deasserted	This pin is asserted	Latched Shutdown

14 Faults and Protections

14.1 Over Current Protection (OCP)

The TDA38640 has two levels of OCP protection: Analog OCP (AOCP) and Digital OCP (DOCP). The AOCP current limit is based on valley inductor current, whereas the DOCP is based on average current information. AOCP is a fast fault response, and should be set to a value that prevents failure of the device.

A novel scheme allows reconstruction of the inductor current from the voltage sensed across the Sync FET Rdson. It should be noted here that it is this reconstructed average inductor current that is digitized by the ADC and used for output current reporting.

The Over current (OC) fault protection circuit also uses the voltage sensed across the RDS (on) of the Synchronous MOSFET; however, the protection mechanism relies on a fast comparator to compare the sensed signal to the overcurrent threshold and does not depend on the ADC or reported current. The current limit scheme uses an internal temperature compensated current source that has the same temperature coefficient as the RDS (on) of the Synchronous MOSFET. As a result, the over-current trip threshold remains almost constant over temperature

The TDA38640 has two levels of OCP protection: Analog OCP (AOCP) and Digital OCP (DOCP). The AOCP current limit is based on valley inductor current, whereas the DOCP is based on average current information. AOCP is a fast fault response, and should be set to a value that prevents failure of the device.

The TDA38640 AOCP can be accessed via three bits in the register map (aocp_thresh_sel [0:2]). The digital OCP (DOCP) is availble via the PMBus register IOUT_OC_FAULT_LIMIT, and the response is decided by IOUT_OC_FAULT_RESPONSE. Available responses are shutdown, retry 6 times and latch off, or retry indefinitely. The indication of the fault is available in STATUS_IOUT register in PMBus.

AOCP shall be enabled during soft-start and normal operation including FCCM and DEM modes. When AOCP is crossed, the low side MOSFET will continue to stay on for the remaining cycle and the following high side pulse will be ignored to allow inductor relaxation (pulse skipping). If an AOCP condition is detected on the rising edge of a PWM pulse, the high side will still be blocked from turning on and the pulse will be skipped.

The high side will continue to be ignored if the current remains above the AOCP threshold. A 10-count counter is implemented to count 10 AOCP events, then a signal is sent to the digital block to perform the programmed response. The counter is reset after 3 consecutive non-OCP events. The count occurs at the valley of the current. Note that COT switching frequency will decrease when skipping pulses. Figure 20 is an example AOCP response.

The TDA38640 also offers cycle-by-cycle AOCP response with eight selectable current limits, which is set by the resistance at ILIM pin. The selected OCP limit bank is loaded to the IC during the power up and cannot be changed on the fly. To change the OCP limit, users must cycle En signal or VCC voltage. Cycle-by-cycle OCP response allows the TDA38640 to fulfill a brief high current demand, such as a high inrush current during the start-up.

The AOCP is activated when En voltage is above its threshold. During AOCP events, the valley of the inductor current is regulated around the AOCP limit. But during the first switching cycle when the AOCP is tripped, the valley of the inductor current can drop slightly below the AOCP limit. It should be noted that AOCP events do not pull the VRRDY signal low unless the output voltage eventually drop below the Under-Voltage Protection (UVP) threshold and trigger UVP.

The OCP limits are thermally compensated. The corresponding output DC current can be calculated as follows:

$$I_{out\_OCP} = I_{LIM} + \frac{\Delta i_L}{2}$$

Faults and Protections

Where: I_{out_OCP} = Output DC current when AOCP is tripped. I_{LIM} = AOCP limit, which is the valley of inductor current. ΔiL = Peak-peak inductor ripple current.

To avoid the inductor saturation during AOCP events, the following criterion is recommended for the inductor saturation current rating.

$$I_{sat} \geq I_{LIM\_max} + \Delta i_L$$

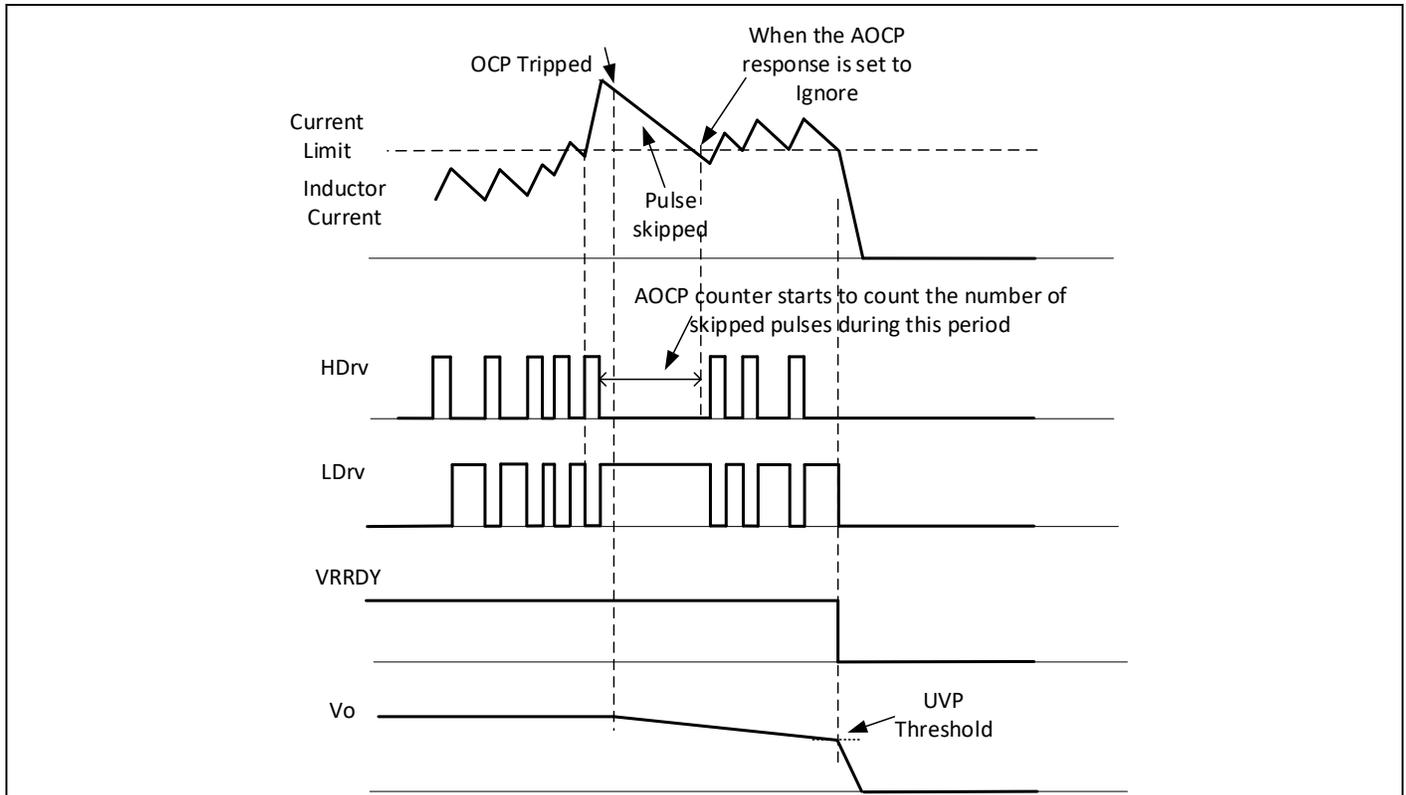Where: I_{sat} is the inductor saturation current and I_{LIM_max} is the maximum spec of the AOCP limit.

Figure 20   AOCP response timing diagram.

14.2   Output Under Voltage Protection (UVP)

The TDA38640 UVP response is a relative limit configurable from 50 mV to 400 mV in steps of 50 mV. The limit is programmed via the VOUT_UV_FAULT_LIMIT PMBus command, and the response is programmed via the VOUT_UV_FAULT_RESPONSE command. There is also the option to program the UVP Limit for the part by accessing the I2C register in the common regmap space. The UVP threshold is enabled using the relative_UVP_thresh_en (0x5E [15]) bit and the levels are set by the relative_uvp_thresh [2:0] (0x5e[10:8]) bits. Possible responses are ignore, shutdown, and retry indefinitely. The relative UVP may be disabled using the disable_relative_UVP(0x60[14]) bit.

When the UVP fault is triggered, a flag is raised and the part is tri-stated until the flag is cleared using the PMBus CLEAR_FAULTS command and the part is started again by either cycling the Vcc or the EN signal to the part. The shutdown response entails tri-stating both the MOSFET's and discharging the output either via a bleed resistor at the output or through the body diode of the low side FET.

If the response is set to retry, a user defined timer (1 ms to 8 ms in steps of 1 ms) is started as soon as the UVP fault is triggered and the output is tri-stated. At the end of the timer the output is checked against a fixed level of 250 mV, if

Faults and Protections

the output is below this voltage the start-up sequence is initiated or else the timer is reset and the output tri-state continues (both the MOSFET's are tri-stated).

There are options for UVP protection to be lifted during voltage transitions (Vboot, DVID up and/or down) using the register bits blank_uv_sel [1:0]. The options for this register are outlined in Table 14.

Table 14   Optional UVP blanking via register blank_uv_sel (0x60[11:10]).

sel	Description
3	blank UV faults during DVID up or down (including Vboot)
2	blank UV faults during DVID up (including Vboot)
1	blank UV faults during Vboot
0	no UV fault blanking

14.3   Over Voltage Protection (OVP)

The OVP response is divided into two parts: Fixed OVP (FOVP) and Relative OVP (ROVP). The Fixed OVP is typically used for start-up, all DVIDs, and when EN is low. ROVP covers all other situations during operation. Figure 21 depicts an example of when FOVP and ROVP are utilized.

The FOVP has 8 distinct levels (0.8 V, 1 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.2 V, and 2.85 V), it is programmable via the configuration fixed_ovp_thresh [2:0] in configuration register 0x60. The response to an OVP event is programmed via the VOUT_OV_FAULT_RESPONSE command. OVP can have four responses: ignore, shutdown, and retry n (max 6) times after n (defined by PMBus) sec before latching and retry foreever. The threshold for ROVP is relative to the programmed output voltage, and can be set from 50 mV to 400 mV in steps of 50mV. The OVP fault can also be blanked by using the bits [13:12] of register 0x60 in common regmap space. Please refer to Table 14 for more details. The threshold for ROVP is relative to the programmed output voltage, and can be set from 50 mV to 400 mV in steps of 50mV using the I2C register relative_ovp_thresh [2:0] (0x5e [14:12]). The PMBUs commands could be over-ridden by using the relative_ovp_thresh_en (0x5e [15]) bit to over-ride the PMBUs commands.

Table 15   Optional OVP balnking via blank_ov_sel(0x60[13:12])

sel	Description
3	blank OV faults during DVID up or down (including Vboot)
2	blank OV faults during DVID up (including Vboot)
1	blank OV faults during Vboot
0	no OV fault blanking

When the output triggers a FOVP event the OVP flag is set, low side switch is turned ON and high side switch is turned OFF. The low side switch is turned ON till the output voltage is dragged down to the set FOVP threshold. After that the output voltage walks down to zero with its natural decay.

When the output triggers an ROVP event, the VID set point is moved to 0V at a controlled slew rate of 30V/uS and the OVP flag is set. Next the low side switch is turned ON and the high side is turned off. This allows the output to discharge until VID set point reaches zero or the Vout cathes up with the VID set point at which point the low side and high side switched turn ON and OFF as required to maintain the output at the VID set point. How fast the output voltage discharges during this event is determined by the by the output voltage, output capacitance and output inductor. This determines if the output voltage indeed is dragged down to zero by the end of the controlled VID ramp down. At the

end of the ramp, if the output is not already dragged down to zero, the output voltage will walk down to zero with its natural decay.
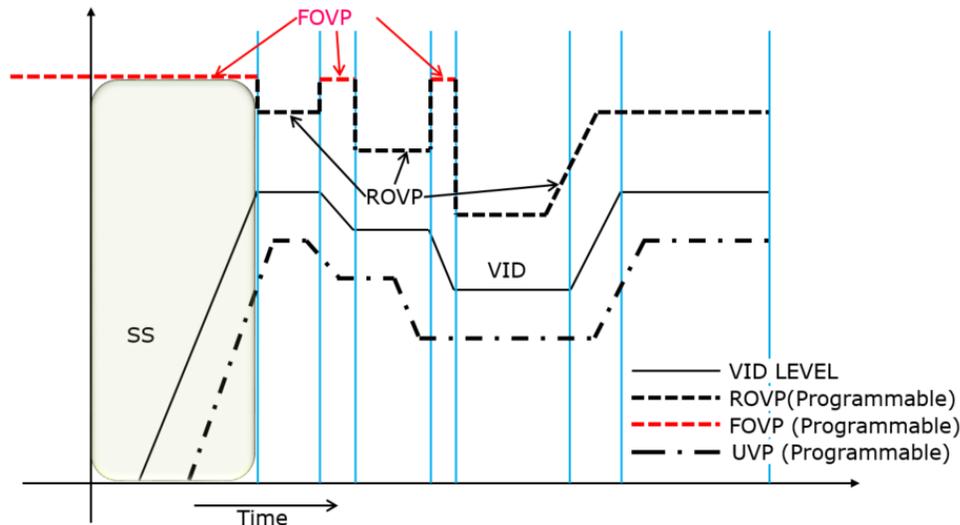
Figure 21   OVP example diagram. Note the situations in which FOVP takes over from ROVP.

14.4   Over Temperature Protection (OTP)

Temperature protection is programmable via the OT_FAULT_LIMIT, OT_WARN_LIMIT, and OT_FAULT_RESPONSE PMBus registers. The TDA38640 supports three responses: ignore, shutdown, and retry idefinitely. The fault is non-latching.

An OTP event is triggered when the device temperature reaches the OT_FAULT_LIMIT. The switching output is tri-stated and the output discharges, while staying biased with the internal LDO on. With the output off, the device cools until reaching the OTP_WARN_LIMIT, and if set to retry, the device will hiccup with potential of pre-biased startup.

14.5   Boot under Voltage Lockout (UVLO)

The voltage from the BOOT pin to PHASE pin is monitored on the TDA38640. If the UVLO Boot lower threshold violation is detected within the PWM cycle, the event is counted and a fault is asserted after 10 violations. After 3 consecutive cycles without a UVLO BOOT event (above the lower threshold during the PWM cycle), the counter resets. To clear the fault Vcc or EN has to be cycled. The Boot UVLO fault is in the fail_code_sticky register.

14.6   Minimum On - Time and Minimum Off - Time

The minimum on-time refers to the shortest time for Control MOSFET to be reliably turned on. The minimum off-time refers to the minimum time duration in which Synchronous FET stays on before a new PWM pulse is generated. The minimum off-time is needed for TDA38640 to charge the bootstrap capacitor, and to sense the current of the Synchronous MOSFET for OCP.

For applications requiring a small duty cycle, it is important that the selected switching frequency results in an on-time larger than the maximum spec of the minimum on-time in the Section **6**. Otherwise the resulting switching

frequency may be lower than the desired target. Following formula could be used to check for the minimum on-time requirement.

$$\frac{V_0}{k f_{sw} \times V_{in}} > \max \; spec \; of \; T_{on(\min)}$$

Where f_{sw} is the desired switching frequency. k is the variation of the switching frequency. As a rule of thumb, select k = 1.25 to ensure the design margin.

For applications requiring a high duty cycle, it is important to make sure a proper switching frequency is selected so that the resulting off-time is longer than the maximum spec of the minimum off-time in the Section **6**, which can be calculated as shown below.

$$\frac{V_{in} - V_0}{k f_{sw} \times V_{in}} > \max \; spec \; of \; T_{off(\min)}$$

Where f_{sw} is the desired switching frequency. k is the variation of the switching frequency. As a rule of thumb, select k = 1.25 to ensure the design margin.

The resulting maximum duty cycle is therefore determined by the selected on-time and minimum off-time.

$$D_{max} = \frac{T_{on}}{T_{on} + T_{off(\min)}}$$

14.7   High-Side Short (HSS) Detection

The TDA38640 offers high-side FET short detection. The phase pin is monitored when the low-side FET is active. HSS monitoring happens both at start-up and during normal operation. In an HSS event, the HSS threshold is reached and both VRRDY and CAT_FAULT# pins are asserted. In the case of an HSS event during start-up, the response is communicated via the CAT_FAULT# pin. Once the HSS threshold is reached, the low-side FET is turned on and the switching stops. There is no current reporting during this time. The fault is sticky and only clears when either the VCC or EN signal is cycled.

15   Faults Communication

TDA38640 supports the the following FAULTs OCP, OVP, UVP, OTP, BOOT UVLO, and Vcc UVLO via telemetry.

15.1   I2C Slave Addressing

The TDA38640 simultaneously supports I2C and PMBus through the use of exclusive addressing. By using a 7-bit address, the user can configure the device to any one of 127 different I2C addresses. Once the address of the TDA38640 is set, it can be locked to protect it from being overridden. Optionally, a resistor can be tied to the SM_ADDR/PROG pin to generate an offset as shown in Table 10 .

 As an example, setting a base 7-bit I2C address of 28h with a resistor offset of +15 sets the 7-bit I2C address to 37h. There is an option to disable the offset functionality on the SM_ADDR pin by using the i2c_disable_addr_offset (0x42[6]) bit from commmon regmap space. When this bit is enabled an offset is added to the base address for i2c depending upon the resistor connected to the SM_ADDR/PROG pin.

Table 16   Disable Offset Options (0x42[6])

Enable I2C_use_addr_offset bit	I2C Address Offset
0	enabled
1	disabled
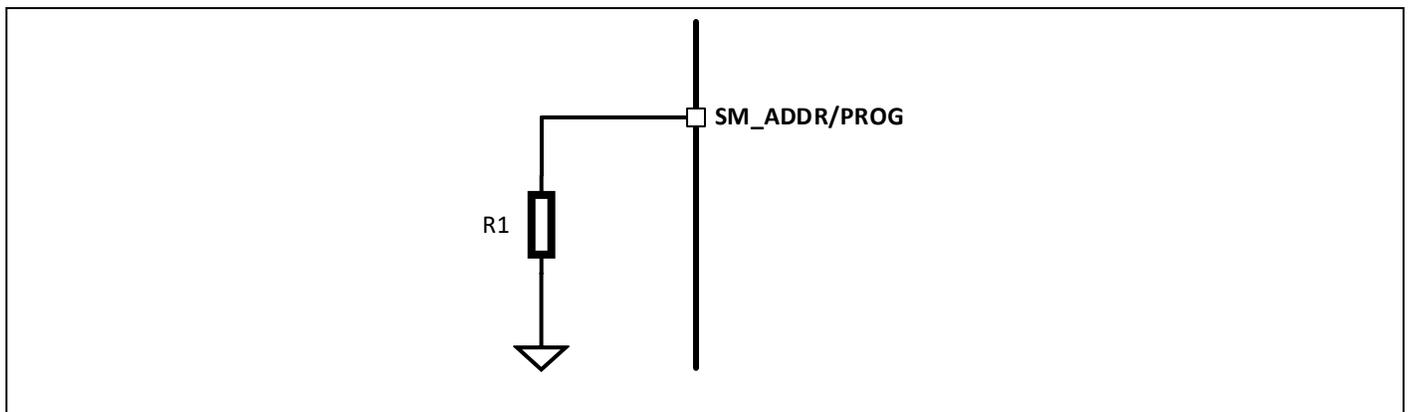
Figure 22   SM-ADDR/PROG Pin Components

15.2   Real-Time Telemetry

TDA38640 provides real-time accurate measurement of input voltage, input current, output voltage, output current temperature, output power, and input power over the I2C interface. Output voltage is calculated based upon the VID setting and the result is reported through the I2C. In SVID domain TDA38640 supports output voltage, output current, input voltage, input current, and input power telemetry.

15.3   I2C Protocol

All registers may be accessed using either I2C or PMBus protocols. I2C allows the use of a simple format whereas PMBus provides error checking capability. Figure 23 shows the I2C format employed by the TDA38640.
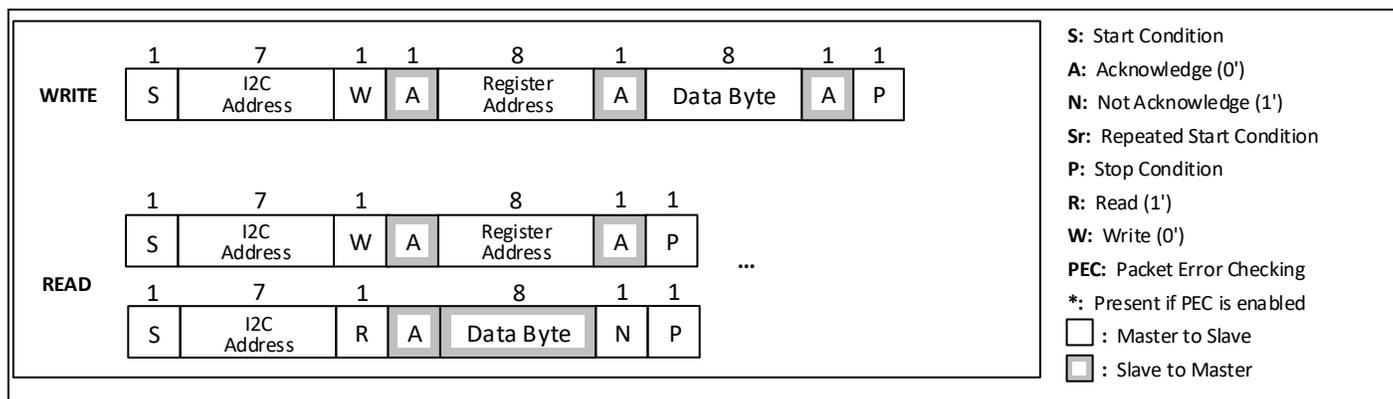
Faults Communication

Figure 23   I2C Format

Table 17   PMBus Commands Supported via I2C

I2C Register Address	COMMAND	PMBus PROTOCOL	PMBus COMMAND CODE	DESCRIPTION
0x200	PAGE	Read/Write Byte	00h	Allows access of each loop via paging.
0x202	OPERATION	Read/Write Byte	01h	Enables or disables the output and controls margining. Ignores OVP on Margin High, UVP on Margin Low.
0x204	ON_OFF_CONFIG	Read/Write Byte	02h	Configures the combination of CONTROL pin and OPERATION command needed to turn the unit on and off.
0x206	CLEAR FAULTS	Send Byte	03h	Clear contents of Fault registers
0x20A	PAGE_PLUS_WRITE	Write Block	05h	Set the PAGE within a device, send a command, and send the data for the command in one packet.
0x20C	PAGE_PLUS_READ	Block Write/ Block Read Process Call	06h	Set the PAGE within a device, send a command, and read the returned data by the command in one packet
0x220	WRITE_PROTECT	Read/Write Byte	10h	Protects from overwriting the configuration files and modes accidentally
0x222	STORE_DEFAULT_ALL	Sen Byte	11h	Instructs the device to copy the entire contents of the configuration registers to the NVM
0x224	RESTORE_DEFAULT_ALL	Send Byte	12h	Reloads the OTP
0x22A	STORE_USER_ALL	Send Byte	15h	Stores the user OTP section
0x22C	RESTORE_USER_ALL	Send Byte	16h	Reloads the user OTP section
0x232	CAPABILITY	Read Byte	19h	Returns 1010xxxx to indicate Packet Error Checking is supported and Maximum bus speed is 400kHz
0x236	SMBALERT_MASK	Block Write/ Block Read Process Call	1Bh	Set to prevent warning or fault conditions from asserting the SMBALERT# signal. Write command code for STATUS register to be masked in the low byte, the bit to be masked in the High byte.

Faults Communication

I2C Register Address	COMMAND	PMBus PROTOCOL	PMBus COMMAND CODE	DESCRIPTION
0x240	VOUT_MODE	Read/Write Byte	20h	Sets the format for VOUT related commands. Linear mode, -8, -9, and -12 exponents supported.
0x242	VOUT_COMMAND	Read/Write Word	21h	Sets the voltage to which the device should set the output. Format according to VOUT_MODE. . Resolution is 5mV when the IC Vout is configured with a load line. Resolution is 5mV or 0.625mV when the IC is configured without a load line.
0x248	VOUT_MAX	Read/Write Word	24h	Sets an upper limit on the output voltage the unit can command. Format according to VOUT_MODE.
0x24A	VOUT_MARGIN_HIGH	Read/Write Word	25h	Sets the margin high voltage when commanded by OPERATION. Must be in format determined by VOUT_MODE.
0x24C	VOUT_MARGIN_LOW	Read/Write Word	26h	Sets the margin low voltage when commanded by OPERATION. Must be in format determined by VOUT_MODE.
0x24E	VOUT_TRANSITION_RATE	Read/Write Word	27h	Sets the rate at which the output changes voltage due to VOUT_COMMAND or OPERATION commands.
0x250	VOUT_DROOP	Read/Write Word	28h	Allows the user to set the load-line value in resolution of 5/256 Ω. Exponent is 1
0x252	VOUT_SCALE_LOOP	Read/Write Word	29h	Used to account for any external attenuation network on VOUT sense feedback and provide correct VOUT reporting.
0x256	VOUT_MIN	Read/Write Word	2Bh	Sets a lower limit on the commanded output voltage. Format according to VOUT_MODE
0x266	FREQUENCY_SWITCH	Read/Write Word	33h	Sets the switching frequency in kHz per table found in user note UN0047. Exp = 0, 1
0x26A	VIN_ON	Read/Write Word	35h	Sets the value of the input voltage at which the unit should begin power conversion. Exp = -1.
0x26C	VIN_OFF	Read/Write Word	36h	Sets the value of the input voltage that the unit, once operation has started, should stop power conversion. Exp = -1.
0x270	IOUT_CAL_GAIN	Read/Write Word	38h	Used to calibrate the output current's gain
0x272	IOUT_CAL_OFFSET	Read/Write Word	39h	Used to null out any offsets in the output current sensing circuitry. Exp = 2.
0x280	VOUT_OV_FAULT_LIMIT	Read Only	40h	Returns the value of the output voltage, measured at the sense or output pins, that causes an output overvoltage fault.
0x282	VOUT_OV_FAULT_RESPONSE	Read/Write Byte	41h	Instructs the device on what action to take in response to an output overvoltage fault. Only shutdown and ignore are supported.
0x288	VOUT_UV_FAULT_LIMIT	Read Only	44h	Returns the value of the output voltage, measured at the sense or output pins, that causes an output undervoltage fault.

Infineon

Faults Communication

I2C Register Address	COMMAND	PMBus PROTOCOL	PMBus COMMAND CODE	DESCRIPTION
0x28A	VOUT_UV_FAULT_ RESPONSE	Read/Write Byte	45h	Instructs the device on what action to take in response to an output undervoltage fault. Only shutdown and ignore are supported.
0x28C	IOUT_OC_FAULT_ LIMIT	Read/Write Word	46h	Sets the value of the output current, in amperes, that causes the overcurrent detector to indicate an overcurrent fault condition. Set by writing this command in Linear format with a -1 exponent.
0x28E	IOUT_OC_FAULT_ RESPONSE	Read/Write Byte	47h	Instructs the device on what action to take in response to an output overcurrent fault. Only C0h (shutdown immediately), F8h (hiccup forever), and D8 (hiccup 3 times) are supported.
0x29E	OT_FAULT_LIMIT	Read/Write Word	4Fh	Sets the temperature, in degrees Celsius, of the unit at which it should indicate an overtemperature fault. Exp = 0.
0x2A0	OT_FAULT_RESPONSE	Read/Write Byte	50h	Instructs the device on what action to take in response to an overtemperature fault. Only shutdown and ignore are supported.
0x2A2	OT_WARN_LIMIT	Read/Write Word	51h	Sets the temperature, in degrees Celsius, of the unit at which it should indicate an Overtemperature Warning alarm. Exp = 0.
0x2AA	VIN_OV_FAULT_LIMIT	Read/Write Word	55h	Sets the value of the input voltage that causes an input overvoltage fault. Exp = -4.
0x2AC	VIN_OV_FAULT_RESPONSE	Read/Write Byte	56h	Instructs the device on what action to take in response to an input overvoltage fault. Only shutdown and ignore are supported.
0x2BC	POWER_GOOD_ON	Read/Write Word	5Eh	Sets the output voltage at which an optional POWER_GOOD signal should be asserted. Format according to VOUT_MODE.
0x2BE	POWER_GOOD_OFF	Read/Write Word	5Fh	Sets the output voltage at which an optional POWER_GOOD signal should be negated. Format according to VOUT_MODE.
0x2C0	TON_DELAY	Read/Write Word	60h	Sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise. Exp = 0.
0x2C2	TON_RISE	Read/Write Word	61h	Sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. Exp = 0.
0x2C8	TOFF_DELAY	Read/Write Word	64h	Sets the time (in ms) from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the unit stops transferring energy to the output. Exp = 0.
0x2CA	TOFF_FALL	Read/Write Word	65h	Sets the time, in milliseconds, from the end of the turn-off delay time until the voltage is commanded to zero. Exp = 0.

Faults Communication

I2C Register Address	COMMAND	PMBus PROTOCOL	PMBus COMMAND CODE	DESCRIPTION
0x2F0	STATUS_BYTE	Read/Write Byte	78h	Returns 1 byte where the bit meanings are: Bit <7> Reserved Bit <6> Output off (due to fault or enable) Bit <5> Output over-voltage fault Bit <4> Output over-current fault Bit <3> Input Under-voltage fault Bit <2> Temperature fault Bit <1> Communication/Memory/Logic fault Bit <0>: None of the Above
0x2F2	STATUS_WORD	Read/Write Word	79h	Returns 2 bytes where the Low byte is the same as the STATUS_BYTE data. The High byte has bit meanings are: Bit <7> Output high or low fault Bit <6> Output over-current fault Bit <5> Input voltage or current fault. Bit <4> MFR_SPECIFIC Bit <3> POWR GOOD# Bit <2:0> Not Supported
0x2F4	STATUS_VOUT	Read/Write Byte	7Ah	Bit <7> Output Overvoltage Fault Bit <6> Not Supported Bit <5> Not Supported Bit <4> Output Undervoltage Fault Bit <3> VOUT_MAX Warning Bit <2:0> Not Supported
0x2F6	STATUS_IOUT	Read/Write Byte	7Bh	Bit <7> Output Overcurrent Fault Bit <6> Not Supported Bit <5> Output Overcurent Warning Bit <4:0> Not Supported
0x2F8	STATUS_INPUT	Read/Write Byte	7Ch	Bit <7> Input Overvoltage Fault Bit <6:0> Not Supported
0x2FA	STATUS_TEMPERATURE	Read/Write Byte	7Dh	Bit <7> Over Temperature Fault Bit <6> Over Temperature Warning Bit <5:0> Reserved
0x2FC	STATUS_CML	Read/Write Byte	7Eh	Returns 1 byte where the bit meanings are: Bit <7> Invalid or unsupported command Bit <6> Invalid or unsupported data Bit <5> PEC fault Bit <4:2> Reserved Bit <1> Other communication fault not listed here

Faults Communication

I2C Register Address	COMMAND	PMBus PROTOCOL	PMBus COMMAND CODE	DESCRIPTION
				Bit <0> Reserved
0x310	READ_VIN	Read Word	88h	Returns the input voltage in Volts
0x312	READ_IIN	Read Word	89h	Returns the input current in Amperes
0x316	READ_VOUT	Read Word	8Bh	Returns the output voltage in the format set by VOUT_MODE
0x318	READ_IOUT	Read Word	8Ch	Returns the output current in Amperes
0x31A	READ_TEMPERATURE_1	Read Word	8Dh	Returns the addressed loop NTC temperature in degrees Celsius
0x32C	READ_POUT	Read Word	96h	Returns the output power in Watts
0x32E	READ_PIN	Read Word	97h	Returns the input power in Watts
0x330	PMBUS_REVISION	Read Byte	98h	Reports PMBus Part I rev 1.1 & PMBUs Part II rev 1.2(draft)
0x332	MFR_ID	Block Read/Write Byte count = 2	99h	The MFR_ID is set to IR (ASCII 52 49) unless programmed differently in the USER registers of the controller.
0x334	MFR_MODEL	Block Read, Byte count = 1	9Ah	The MFR_MODEL is the same as the device ID if the USER register for Manufacturer model is 00. Otherwise MFR_Model command returns the value in the USER register for MFR_MODEL.
0x336	MFR_REVISION	Block Read, Byte count = 2	9Bh	The MFR_REVISION is the same as the device revision if the USER register for Manufacturer revision is 00. Otherwise MFR_REVISION command returns the value in the USER register for MFR_REVISION.
0x35A	IC_DEVICE_ID	Block Read	ADh	Returns a 1-byte code with the following values: 5Dh = TDA38640
0x35C	IC_DEVICE_REV	Block Read	AEh	The IC revision that is stored inside the IC
0x3A0	MFR_READ/WRITE_ REG	Custom MFR protocol	D0h	Read/Write I2C registers

15.4   11-BIT Linear Data Format

Monitored parameters use the Linear Data Format (Figure 24) encoding into 1 Word (2 bytes), where:

$$Value = Y * 2^N$$

Note N and Y are "signed" values. If VOUT is set to linear format (by VOUT_MODE), then N is set by the VOUT_MODE command and only Y is returned in the data-field as a 16-bit unsigned number.
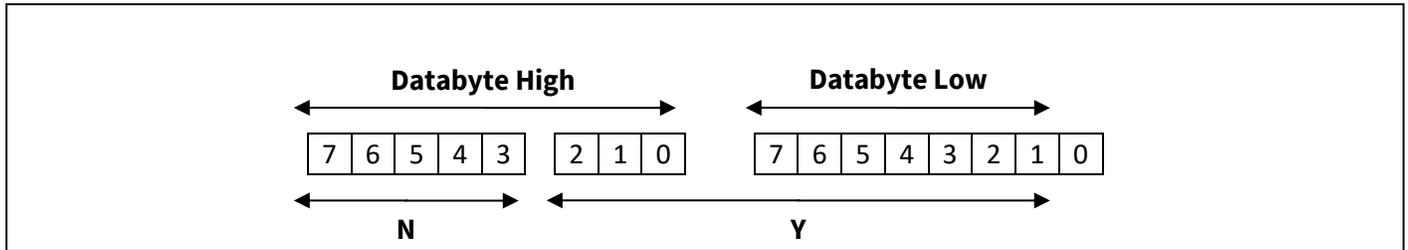
Figure 24   11-Bit Linear Data Format

15.5   16-BIT Linear Data Format

This format is only used for VOUT related commands (READ_VOUT, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, POWER_GOOD_ON, and POWER_GOOD_LOW):

$$Value = Y * 2^N$$

Note N and Y are "signed" values. If VOUT is set to linear format (by VOUT_MODE), then N is set by the VOUT_MODE command and only Y is returned in the data-field as a 16-bit unsigned number.
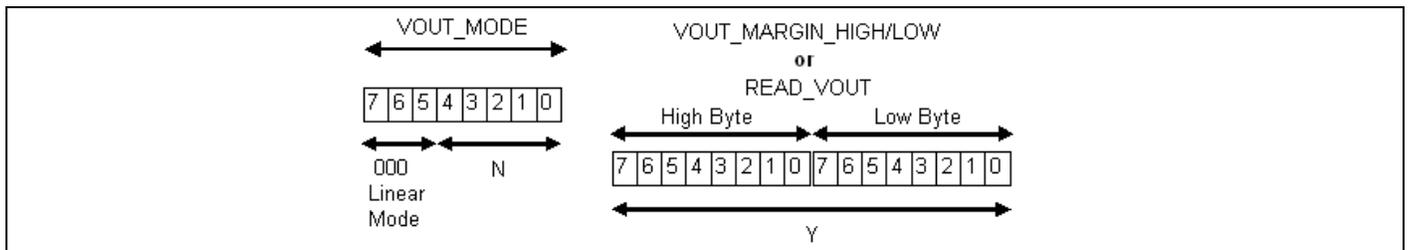
Figure 25   16-BIT Linear Data Format

15.6   SVID Registers

A list of all the SVID registers is given in Table 18. SVID registers supported by TDA38640 in VR12.5, VR13, and VR13.HC mode conform to VR12.5, VR13, and VR13.HC specifications respectively.

Table 18   SVID Registers

Register Address	Register Name	Access	VR12.5 Mode	VR13 Mode	VR14 Mode
00	Vendor ID	RO	Supported	Supported	Supported
01	Product ID	RO	Supported	Supported	Supported
02	Product Revision	RO	Supported	Supported	Supported
03	Product Date Code	-	Not Supported	Not Supported	Not Supported
04	Lot Code	-	Not Supported	Not Supported	Not Supported
05	Protocol ID	RO	Supported	Supported	Supported

Faults Communication

Register Address	Register Name	Access	VR12.5 Mode	VR13 Mode	VR14 Mode
06	Capability	RO	Supported	Supported	Supported
07	Step Size	RO	Not Supported	Not Supported	Not Supported
07	Vendor Use	RW	Not Supported	Not Supported	Not Supported
08	Bias VID Table	RO	Not Supported	Not Supported	Not Supported
09	VIDOMAX_H_CAPA	RO	Not Supported	Not Supported	Supported
0A	VIDOMAX_L	RO	Not Supported	Not Supported	Supported
0B	VIN_FULLSCALE_H	RO	Not Supported	Not Supported	Not Supported
0C	VIN_FULLSCALE_L	RO	Not Supported	Not Supported	Not Supported
0D	VOUT_FULLSCALE_H	RO	Not Supported	Not Supported	Supported
0E	VOUT_FULLSCALE_L	RO	Not Supported	Not Supported	Supported
0F	ALLCALL_ACT	RW	Not Supported	Not Supported	Supported
10	Status_1	RO	Supported	Supported	Supported
11	Status_2	RO	Supported	Supported	Supported
12	Temperature	RO	Supported	Supported	
13	PMIC_GLOBAL_ST	RO	Not Supported	Not Supported	Not Supported
14	LASTREAD	RO	Not Supported	Not Supported	Supported
15	IOUT_H	RO	Supported	Supported	Supported
16	VOUT_H	RO	Supported	Supported	Supported
17	VR Temperature	RO	Supported	Supported	Supported
18	Output Power	RO	Supported	Supported	Supported
19	Input Current	RO	Not Supported	Not Supported	Not Supported
1A	Input Voltage	RO	Not Supported	Not Supported	Not Supported
1B	Input Power	RO	Not Supported	Not Supported	Not Supported
1C	Status 2 Last Read	RO	Supported	Supported	Supported

Faults Communication

Register Address	Register Name	Access	VR12.5 Mode	VR13 Mode	VR14 Mode
1D	PARERR_CNT	RO	Not Supported	Not Supported	Not Supported
1E	CFG_FILE_ID	RO	Not Supported	Not Supported	Supported
1F	Future Command	-	Not Supported	Not Supported	Not Supported
20	ICC IN Max	RO	Not Supported	Not Supported	Not Supported
21	ICC Max	RO	Supported	Supported	Supported
22	Temp Max	RO	Not Supported	Supported	Supported
23	DC_LL	RO	Not Supported	Not Supported	Not Supported
24	SR_Fast	RO	Supported	Supported	Supported
25	SR_Slow	RO	Supported	Supported	Supported
26	Vboot	RO	Supported	Supported	Supported
27	VR Tolerance	-	Not Supported	Not Supported	Not Supported
28	Current-Offset	RW	Not Supported	Not Supported	Not Supported
29	Temperature Offset	RW	Not Supported	Not Supported	Not Supported
2A	Slow Slew Rate Select	RW	Not Supported	Supported	Supported
2B	PS4 Exit Latency	RO	Not Supported	Not Supported	Supported
2C	PS3 Exit Latency	RO	Not Supported	Not Supported	Supported
2D	Enable to Ready	RO	Not Supported	Not Supported	Supported
2E	Pin Max	RO	Not Supported	Not Supported	Not Supported
2F	Pin Alert Threshold	RW	Not Supported	Not Supported	Not Supported
30	V_{OUT} Max	RW	Supported	Supported	Supported
31	VID Setting	RW	Supported	Supported	Supported
32	Pwr State	RW	Supported	Supported	Supported
33	Offset	RW	Supported	Supported	Supported
34	Multi VR Config	RW	Supported	Supported	Supported

Faults Communication

Register Address	Register Name	Access	VR12.5 Mode	VR13 Mode	VR14 Mode
35	MAIN_ADDR_PTR	RW	Not Supported	Not Supported	Not Supported
36	DC_LL_FINE	RO	Not Supported	Not Supported	Not Supported
37	Future Command	-	Not Supported	Not Supported	Not Supported
38	Future Command	-	Not Supported	Not Supported	Not Supported
39	Future Command	-	Not Supported	Not Supported	Not Supported
3A	Work Point 0	RW	Not Supported	Supported	Supported
3B	Work Point 1	RW	Not Supported	Supported	Supported
3C	Work Point 2	RW	Not Supported	Supported	Supported
3D	Work Point 3	RW	Not Supported	Supported	Supported
3E	Work Point 4	RW	Not Supported	Not Supported	Not Supported
3F	Work Point 5	RW	Not Supported	Not Supported	Not Supported
40	Work Point 6	RW	Not Supported	Not Supported	Not Supported
41	Work Point 7	RW	Not Supported	Not Supported	Not Supported
42	IVID1-VID	RW	Not Supported	Not Supported	Not Supported
43	IVID1-I	RW	Not Supported	Not Supported	Not Supported
44	IVID2-VID	RW	Not Supported	Not Supported	Not Supported
45	IVID2-I	RW	Not Supported	Not Supported	Not Supported
46	IVID3-VID	RW	Not Supported	Not Supported	Not Supported
47	IVID3-I	RW	Not Supported	Not Supported	Not Supported
50	HIGH_PWR	RO	Not Supported	Not Supported	Supported

Faults Communication

Register Address	Register Name	Access	VR12.5 Mode	VR13 Mode	VR14 Mode
51	PWRSTATE_SUP	RO	Not Supported	Not Supported	Supported
52	PHSHED_SUP	RO	Not Supported	Not Supported	Supported
53	PHSHED_ACT	RW	Not Supported	Not Supported	Supported
54	NEGVREN_SUP	RO	Not Supported	Not Supported	Supported
55	NEGVREN_ACT	RW	Not Supported	Not Supported	Supported
56	DIGOUT_STATUS	RO	Not Supported	Not Supported	Not Supported
57	WP_SLEW_0	RW	Not Supported	Not Supported	Supported
58	WP_SLEW_1	RW	Not Supported	Not Supported	Supported
59	WP_SLEW_2	RW	Not Supported	Not Supported	Not Supported
5A	WP_SLEW_3	RW	Not Supported	Not Supported	Not Supported
5B	WP_SLEW_TT	RW	Not Supported	Not Supported	Supported
60	CAL_CAPABILITY	RO	Not Supported	Not Supported	Not Supported
61	CAL_REQUEST	WT	Not Supported	Not Supported	Not Supported
62	CAL_IMAG_A	RW	Not Supported	Not Supported	Not Supported
63	CAL_IMAG_B	RW	Not Supported	Not Supported	Not Supported
64	CAL_STATUS	RO	Not Supported	Not Supported	Not Supported
70	EXP_ACCURACY	RO	Not Supported	Not Supported	Not Supported
71	IOUT_L	RO	Not Supported	Not Supported	Not Supported
72	VOUT_L	RO	Not Supported	Not Supported	Not Supported
73	POUT_L	RO	Not Supported	Not Supported	Not Supported

Faults Communication

Register Address	Register Name	Access	VR12.5 Mode	VR13 Mode	VR14 Mode
74	IIN_L	RO	Not Supported	Not Supported	Not Supported
75	VIN_L	RO	Not Supported	Not Supported	Not Supported
76	PIN_L	RO	Not Supported	Not Supported	Not Supported
77	PSYS_CR_LVL_L	RW	Not Supported	Not Supported	Not Supported
78	PSYS_W2_LVL_L	RW	Not Supported	Not Supported	Not Supported
79	PSYS_W1_LVL_L	RW	Not Supported	Not Supported	Not Supported
7A-BF	RESERVED		Not Supported	Not Supported	Not Supported
C0-FF	VENDOR_RESERVED	RW	Not Supported	Not Supported	Not Supported

16 Design example

In this section, an example is used to explain how to design a buck regulator with the TDA38640. The application circuit with the test results are shown in the user guide of the Eval board for TDA38640. The design specifications are given below.

- PV_{in} = 12 V (±10%)
- V_o = 1.0 V
- I_o = 40 A
- V_o ripple voltage = ±1% of V_o
- Load transient response = ± 3% of V_o with a step load current = 9 A and slew rate = 30 A/μs

16.1 Enabling the TDA38640

The TDA38640 has a precise Enable threshold voltage, the Enable feedback resistor, R_{EN1} and R_{EN2}, can be calculated as follows.

$$PV_{in(\min)} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \geq V_{EN(\max)}$$

$$R_{EN2} \geq R_{EN1} \times \frac{V_{EN(\max)}}{PV_{in(\min)} - V_{EN(\max)}}$$

Where $V_{EN(max)}$ is the maximum spec of the En-start-threshold as defined in the Absolute Maximum Ratings table. For $PV_{in\ (min)}$=10.8 V, select R_{EN1}=49.9 kΩ and R_{EN2}=7.5 kΩ.

16.2 Programming the Switching Frequency and Operation Mode

The TDA38640 has very good efficiency performance and is suitable for high switching frequency operation. In this case, 800 kHz is selected to achieve a good compromise between the efficiency, passive component size and dynamic response. In addition, FCCM operation is selected to ensure a small output ripple voltage over the entire load range. 800 kHz switching frequency and FCCM operation can be selected via register bits.

16.3 Selecting Input Capacitors

Without input capacitors, the pulse current of Control MOSFET is directly from the input supply power. Due to the impedance on the cable, the pulse current can cause disturbance on the input voltage and potential EMI issues. The input capacitors filter the pulse current, resulting in almost constant current from the input supply. The input capacitors should be selected to tolerate the input pulse current, and to reduce the input voltage ripple. The RMS value of the input ripple current can be expressed by:

$$I_{RMS} = I_o \times \sqrt{D \times (1 - D)}$$

$$D = \frac{V_o}{PV_{in}}$$

Design example

Where I_{RMS} is the RMS value of the input capacitor current. I_o is the output current and D is the Duty Cycle. For $I_o = 40A$ and $D_{(max)} = 0.09$, the resulting RMS current flowing into the input capacitor is $I_{rms} = 11.6$ A.

To meet the requirement of the input ripple voltage, the minimum input capacitance can be calculated as follows.

$$C_{in(\text{min})} > \frac{I_o \times (1 - D) \times D}{f_{sw} \times (\Delta PV_{in} - ESR \times I_o \times (1 - D))}$$

Where ΔPV_{in} is the maximum allowable peak-to-peak input ripple voltage, and ESR is the equivalent series resistor of the input capacitors. Ceramic capacitors are recommended due to low ESR, ESL and high RMS current capability. For $I_o = 40$ A, $f_{sw} = 800$ kHz, ESR = 3 mΩ, and $\Delta PV_{in} = 240$ mV, $C_{in(min)} > 32$ μF. To account for the de-rating of ceramic capacitors under a bias voltage, 10 x 22 μF/0805/25V MLCC are used for the input capacitors. In addition, a bulk capacitor is recommended if the input supply is not located close to the voltage regulator.

16.4 Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value results in a large ripple current, lower efficiency and high output noise, but helps with size reduction and transient load response. Generally, the desired peak-to-peak ripple current in the inductor (Δi) is found between 20% and 50% of the output current.

The inductor saturation current must be higher than the maximum spec of the OCP limit plus the peak-to-peak inductor ripple current. For some core material, inductor saturation current may decrease as the increase of temperature. So, it is important to check the inductor saturation current at the maximum operating temperature.

The inductor value for the desired operating ripple current can be determined using the following relation:

$$L = (PV_{in(\text{max})} - V_o) \times \frac{D_{min}}{\Delta i_{L(\text{max})} \times F_{sw}}$$

$$D_{min} = \frac{V_o}{PV_{in(\text{max})}}$$

$$I_{sat} \geq OCP_{max} + \Delta i_{L(\text{max})}$$

Where: $PV_{in(max)}$ = Maximum input voltage; ΔiL_{max} = Maximum peak-to-peak inductor ripple current; OCP_{max} = maximum spec of the OCP limit as defined in Section 14.1, and I_{sat} = inductor saturation current. In this case, select inductor L =150 nH to achieve $\Delta iL_{max} = 25\%$ of I_{omax}. The I_{sat} should be no less than 56 A.

16.5 Output Capacitor Selection

The output capacitor selection is mainly determined by the output voltage ripple and transient requirements.

To satisfy the V_o ripple requirement, C_o should satisfy the following criterion.

$$C_o > \frac{\Delta i_{Lmax}}{8 \times \Delta V_{or} \times f_{sw}}$$

Where ΔV_{or} is the desired peak-to-peak output ripple voltage. For $\Delta iL_{max} = 7.5$ A, $\Delta V_{or} = 20$ mV, $f_{sw} = 800$ kHz, C_o must be larger than 59 μF. The ESR and ESL of the output capacitors, as well as the parasitic resistance or inductance due to PCB layout, can also contribute to the output voltage ripple. It is suggested to use Multi-Layer Ceramic Capacitor (MLCC) for their low ESR, ESL and small size.

To meet the transient response requirements, the output capacitors should also meet the following criterion.

Design example

$$C_o > \frac{L \times \Delta I_{o(\max)}^2}{2 \times \Delta V_{oL} \times V_o}$$

Where ΔV_{OL} is the allowable V_o deviation during the load transient. $\Delta I_{o(max)}$ is the maximum step load current. Please note that the impact of ESL, ESR, control loop response, transient load slew rate, and PWM latency is not considered in the calculation shown above. Extra capacitance is usually needed to meet the transient requirements. As a rule of thumb, we can triple the C_o that is calculated above as a starting point, and then optimize the design based on the bench measurement. In this case, to meet the transient load requirement (i.e. ΔV_{OL}= 30 mV, $\Delta I_{o(max)}$ = 9 A), select C_o = ~600 µF. For more accurate estimation of C_o, simulation tool should be used to aid the design.

16.6 Output Voltage Programming

Output voltage can be programmed with register bits and modified with PMBus or SVID commands, depending on chosen operating mode.

16.7 Bootstrap Capacitor

For most applications, a 0.1 µF ceramic capacitor is recommended for bootstrap capacitor placed between PHASE and BOOT Pin. For applications requiring PV_{in} equal to or above 14 V, a small resistor of 1~2 Ω should be used in series with the BOOT pin to ensure the maximum SW node spike voltage does not exceed 20 V.

16.8 VIN, and VCC/LDO bypass Capacitor

Please see the recommendation in 13.4 on the internal LDO. A 10 µF MLCC is selected for VCC/LDO bypass capacitor and a 4.7 µF MLCC is selected for VIN bypass capacitor.

17 Layout Recommendations

PCB layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results. Following design guidelines are recommended to achieve the best performance.

- Bypass capacitors, including input/output capacitors Vcc/VDRV bypass capacitors, should be placed near the corresponding pins as close as possible.
- Place bypass capacitors from TDA38640 power input (Drain of Control MOSFET) to PGND (Source of Synchronous MOSFET) to reduce noise and ringing in the system. The output capacitors should be terminated to a ground plane that is away from the input PGND to mitigate the switching spikes on the Vo. The bypass capacitor shared by VCC and VDRV should be terminated to PGND.
- Place a boot strap capacitor near the TDA38640 BOOT and PHASE pin as close as possible to minimize the loop inductance.
- SW node copper should only be routed on the top layer to minimize the impact of switching noises
- Connect AGND pin to the PGND pad through a single point connection. On the TDA38640 demo board, AGND pin is connected to the exposed PGND pad with a copper trace.
- Via holes can be placed on PVin and PGND pads to aid thermal dissipation.
- Wide copper polygons are desired for PVin and PGND connections in favor of power losses reduction and thermal dissipation. Sufficient via holes should be used to connect power traces between different layers.
- Output voltage sensing in TDA38640 is done differentially using the VOSENP and VOSENM pins.
  - A pair of PCB traces with at least 15 mil trace width, running close to each other and away from any noise sources such as inductor and SW nodes, should be used to implement Kelvin sensing of the voltage across a high-frequency bypass capacitor of 0.1 µF or higher.
  - The ground connection of the remote sensing signal must be terminated at VOSENM pin.
  - The Vo connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor terminated at VOSENM pin for output voltages greater than 2.5 V.
  - Shield the pair of remote sensing lines with ground planes above and below
  - Do **NOT** connect VOSENM pin and AGND pin in this configuration
- VINSENM and VINSENP lines have to be routed differentially and they should be shielded with ground planes from above and below
- For routing the SVID lines Intel's guidance on the spacing and length of the lines allowed (maximum) should be followed. One should also pay attention to the matching resistors and the pull-up requirements when routing these lines to multiple SVID slaves. All of this information is available in the Intel VR14 PWM spec document.
- The En pin and configuration pins including SM_ADDRS/PROG should be terminated to a quiet ground. On the TDA38640 standard demo board, they are terminated to the PGND copper plane away from the power current flow. Alternatively, they can be terminated to a dedicated AGND PCB trace.

More information about the layout is found in the USER guide for the Eval Board for TDA38640. For more information on it please get in touch with the respective Sales team member.

17.1 PCB Metal and Component Placement

Evaluation has shown that the best overall performance is achieved using the substrate/PCB layout as shown in the following figures. PQFN devices should be placed to an accuracy of 0.050 mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

Layout Recommendations

For further information, please refer to "SupIRBuck™ Multi-Chip Module (MCM) Power Quad Flat No-Lead (PQFN) Board Mounting Application Note." (AN1132)
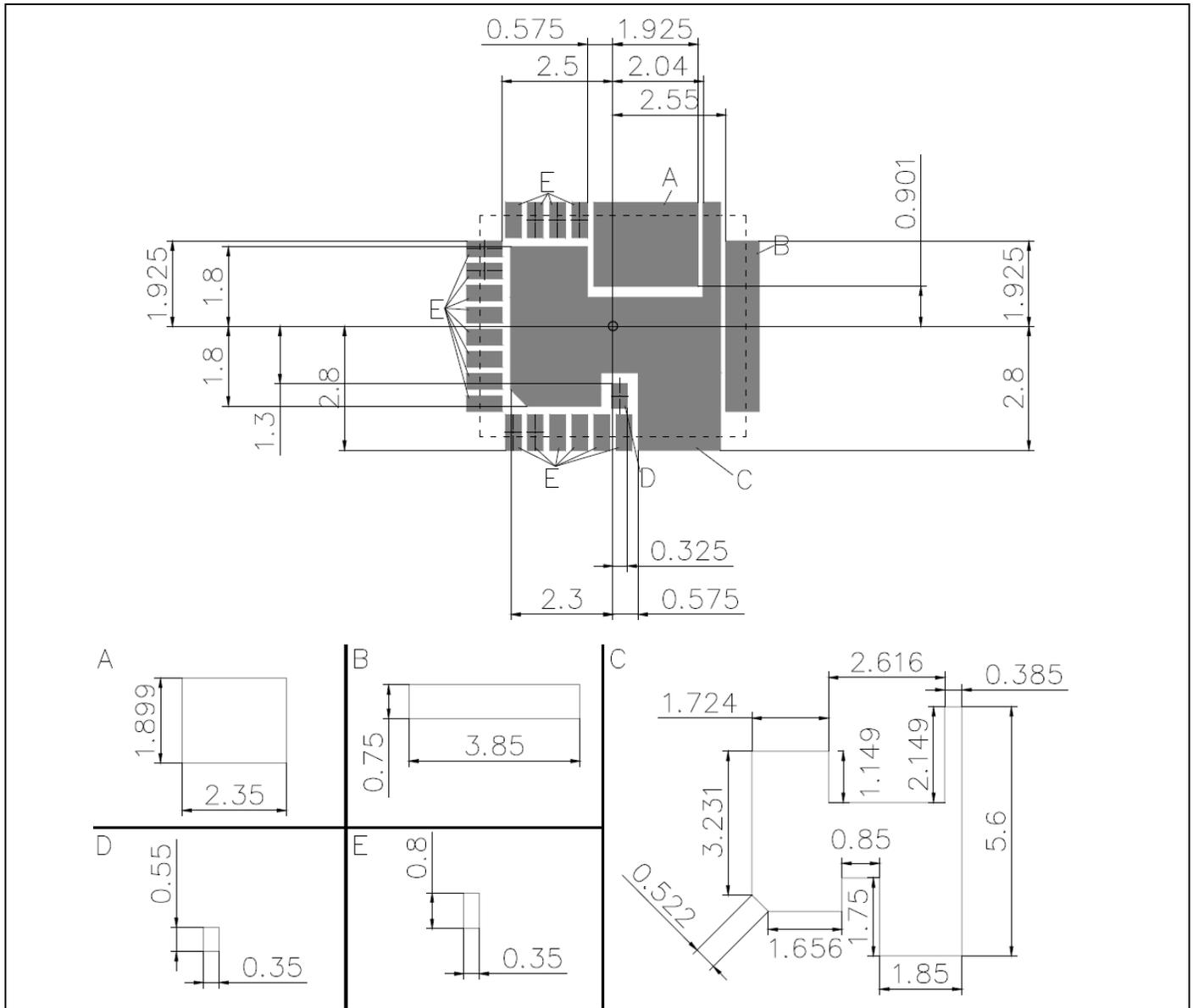
Figure 26   PCB metal pad sizing and spacing (all dimensions in mm)

17.2   Solder Resist

Infineon recommends that larger Power or Land Area pads are Solder Mask Defined (SMD.) This allows the underlying copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05 mm larger (on each edge) than the Solder Mask window, in order to accommodate any layer to layer misalignment. (i.e. 0.1 mm in X & Y.) When using NSMD pads, the Solder Resist Window should be larger than the Copper Pad by at least 0.025 mm on each edge, (i.e. 0.05 mm in X&Y,) in order to accommodate any layer to layer misalignment. Ensure that the solder resist in-between the smaller signal lead areas is at least 0.15 mm wide, due to the high x/y aspect ratio of the solder mask strip.
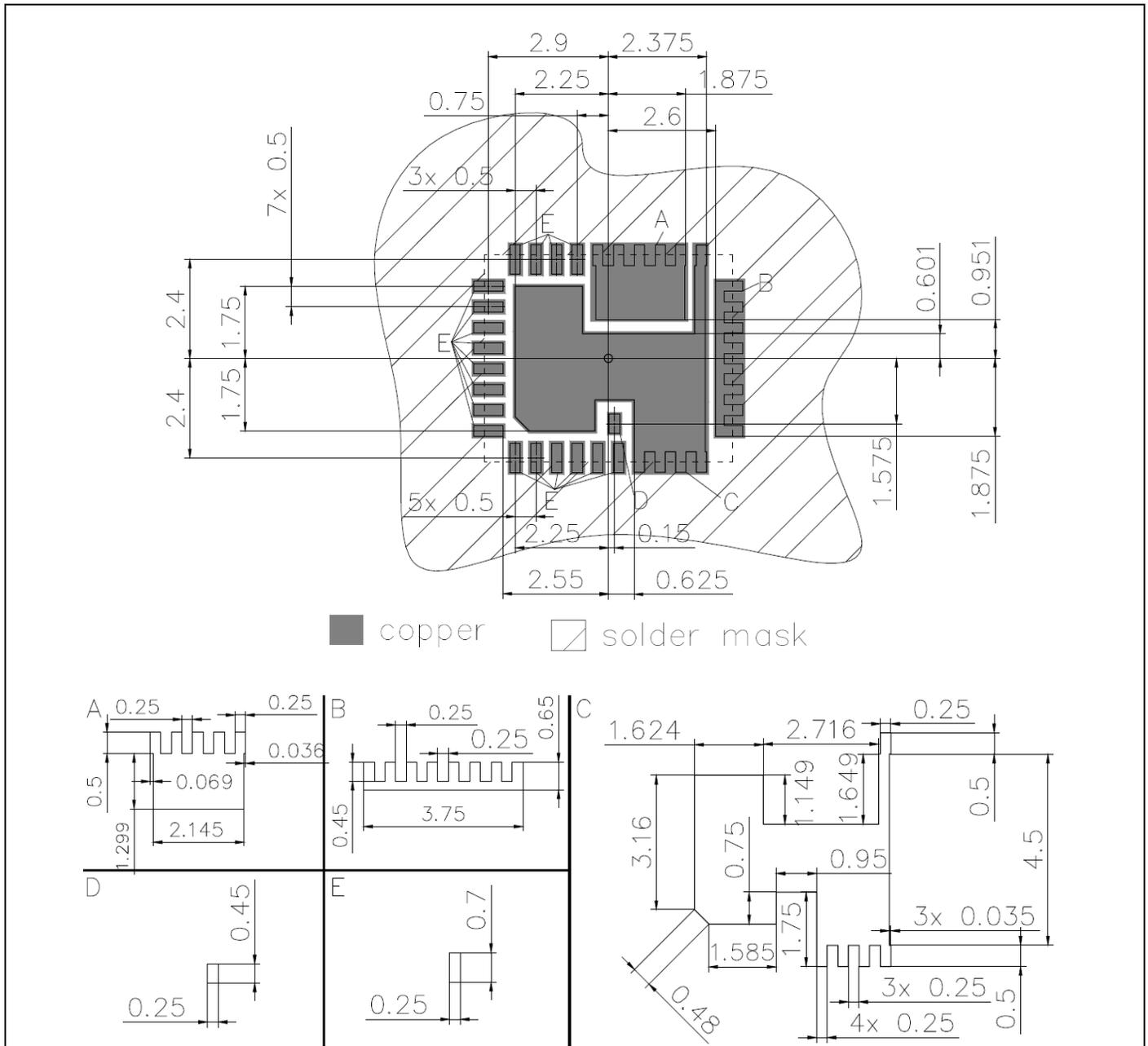
Figure 27   Solder resist

17.3   Stencil Design

Stencils for PQFN packages can be used with thicknesses of 0.100-0.250 mm (0.004-0.010"). Stencils thinner than 0.100 mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125 mm-0.200 mm (0.005-0.008"), with suitable reductions, give the best results.

A recommended stencil design is shown in Figure 28. This design is for a stencil thickness of 0.127 mm (0.005"). The reduction should be adjusted for stencils of other thicknesses.

Layout Recommendations
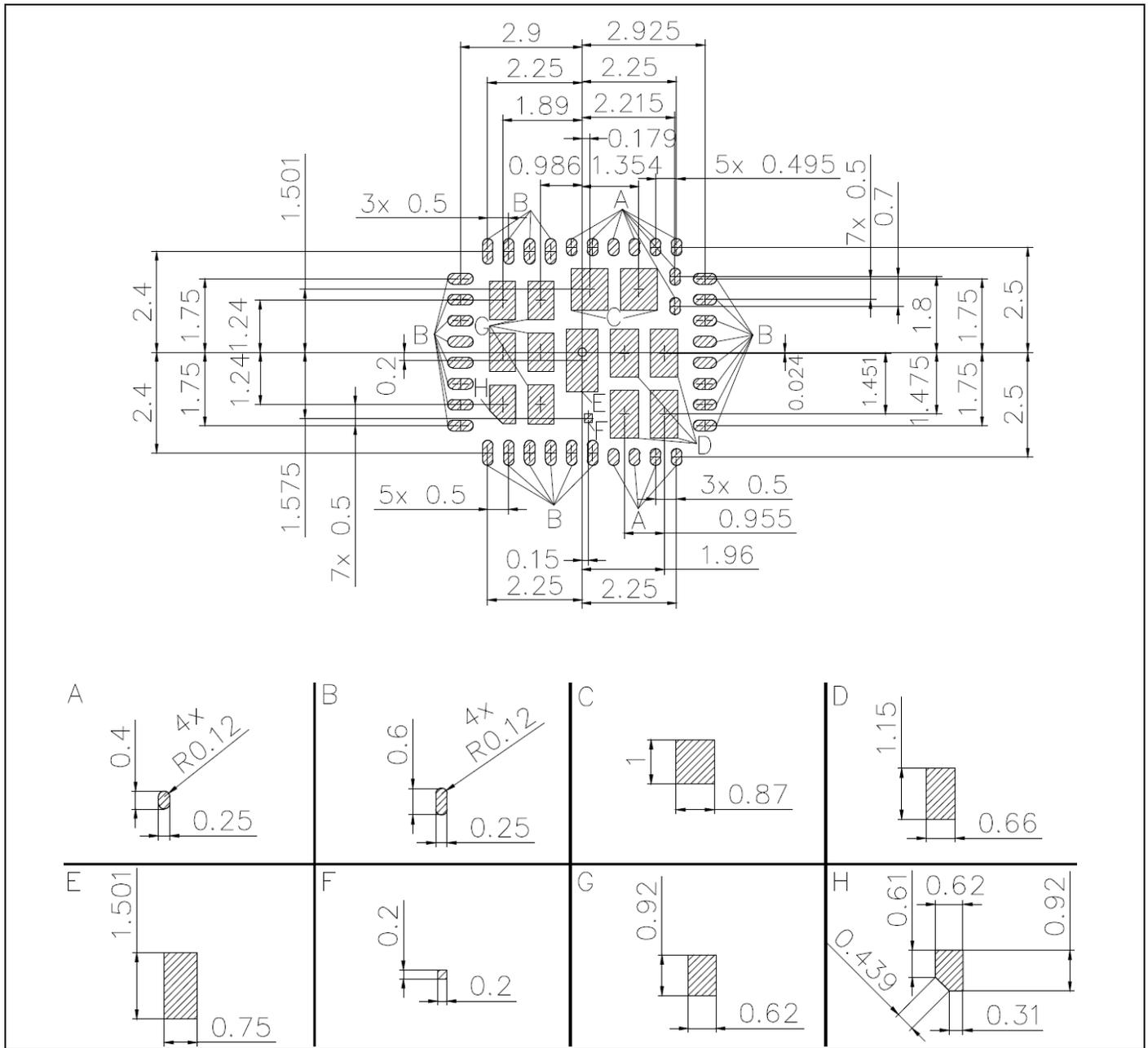
Figure 28 Stencil pad size and spacing (all dimensions in mm)

18 Package

18.1 Marking Information
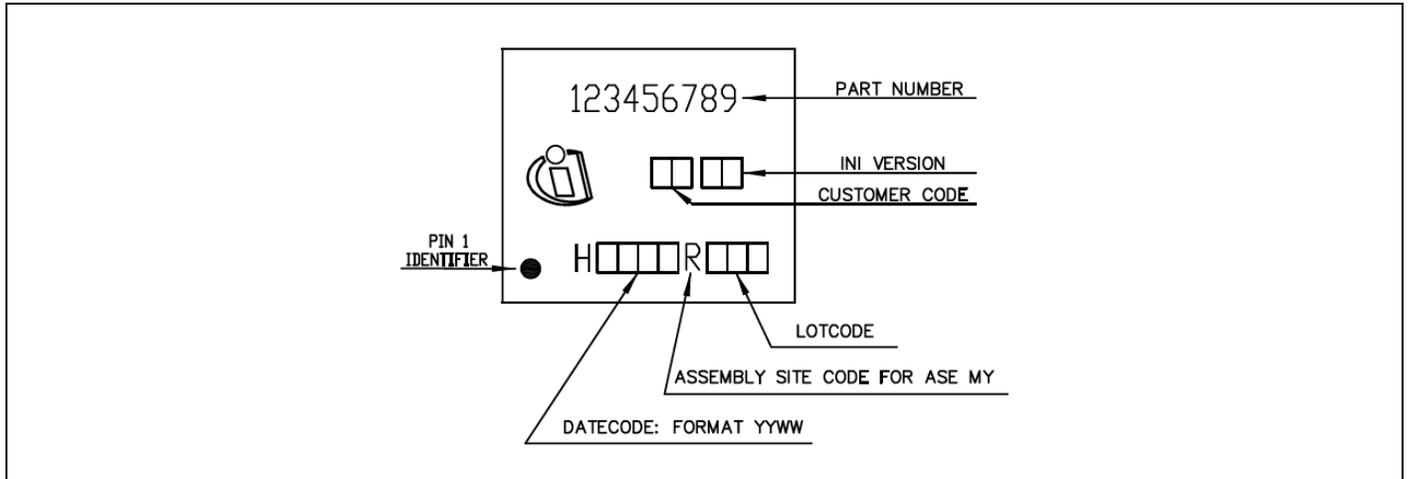
Figure 29   Package Marking

18.2 Dimensions
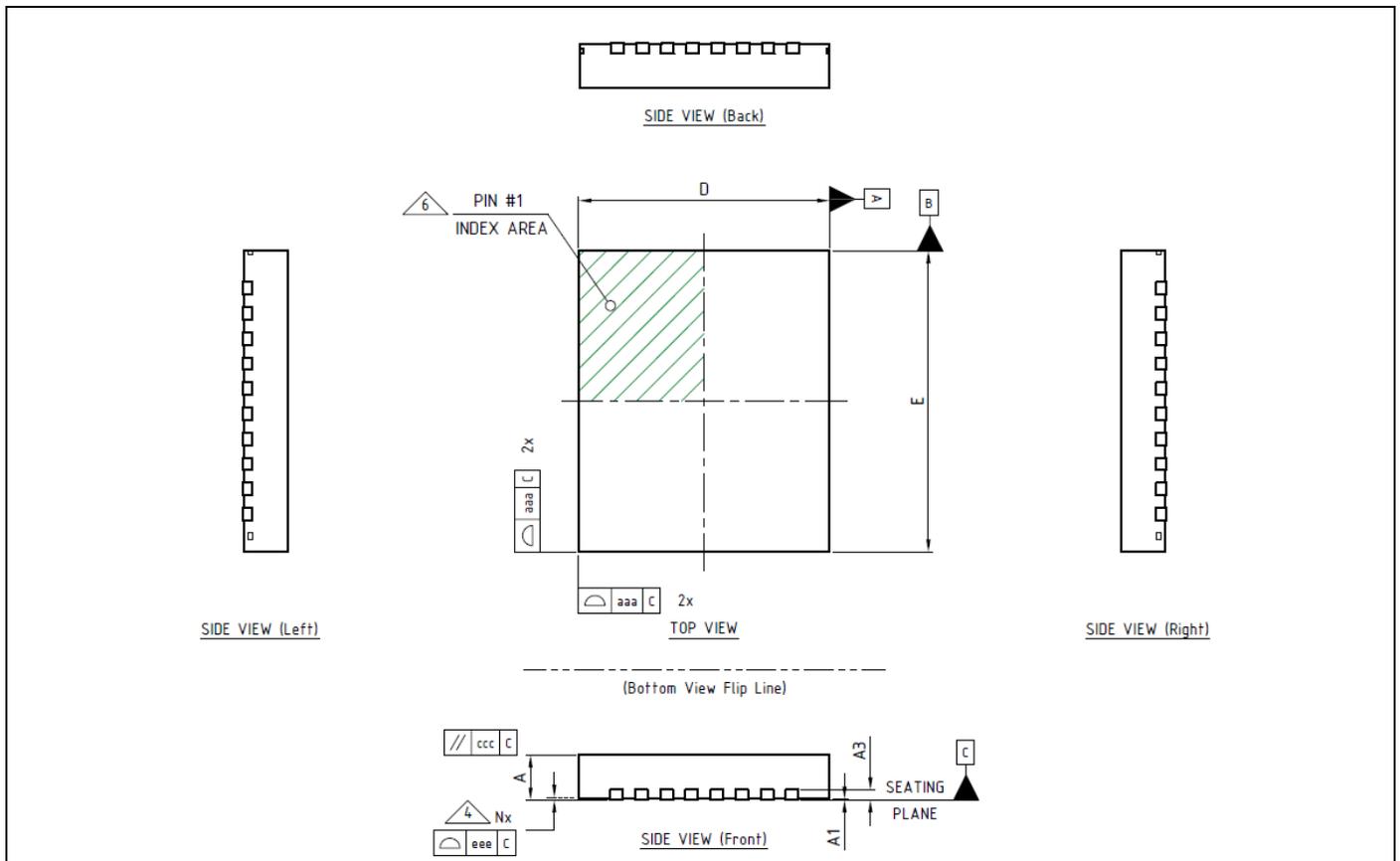
Figure 30   Package view

Package

Thickness Symbol	V			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
A3	---	0.20 Ref	---	
b	0.20	0.25	0.30	5
D	4.90	5.00	5.10	
D1	2.750	2.850	2.950	
D2	3.40	3.50	3.60	
D3	1.199	1.299	1.399	
D4	1.500	1.600	1.700	
E	5.90	6.00	6.10	
E1	1.615	1.715	1.815	
E2-1	1.825	1.925	2.025	
E2-2	1.524	1.624	1.724	
E3	2.045	2.145	2.245	
L	0.35	0.40	0.45	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		36		3
NOTES		1, 2		
LF PART NO.		T B A		
LF DWG. NO.		T B A		
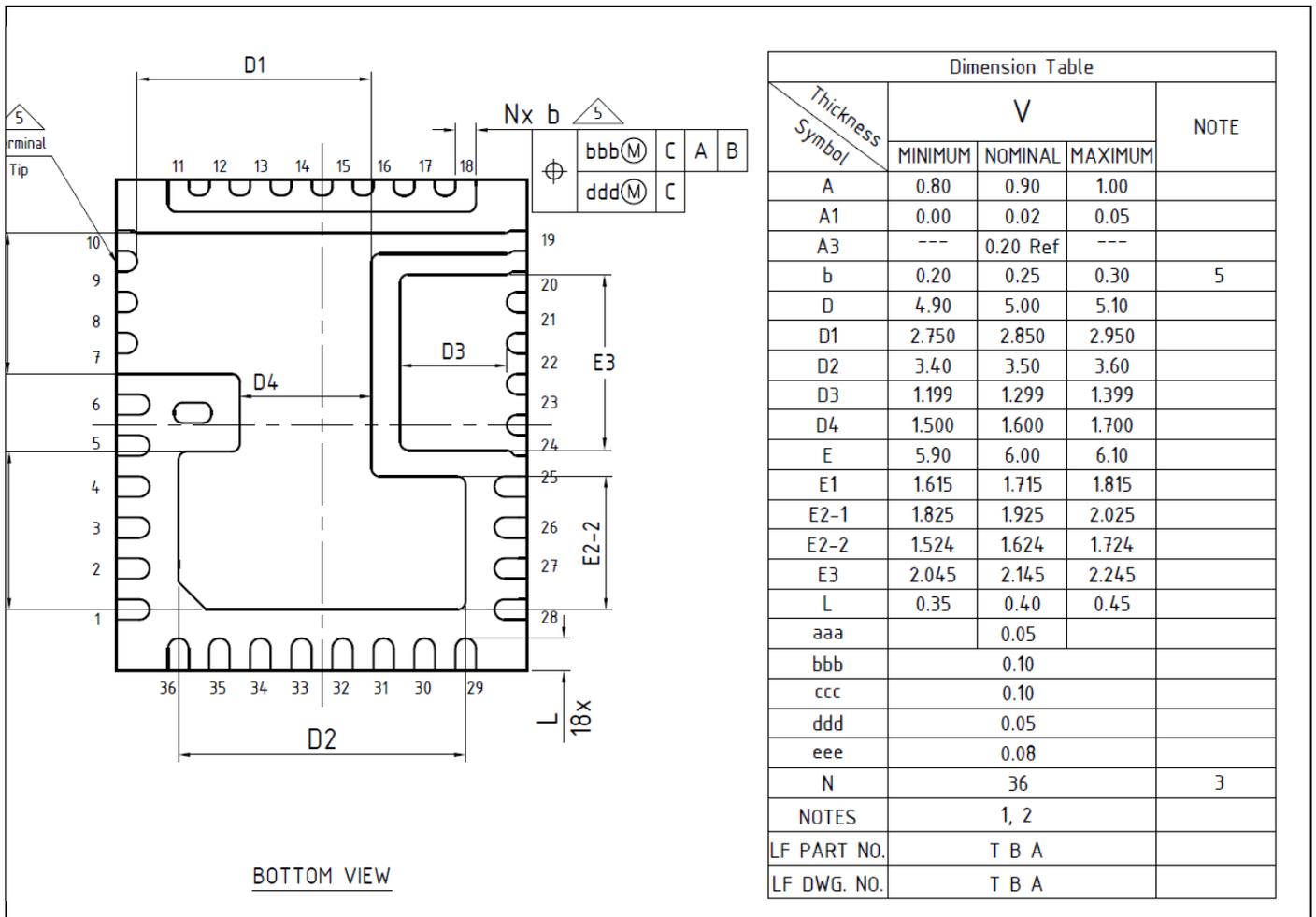
Figure 31   Package Dimensions in mm
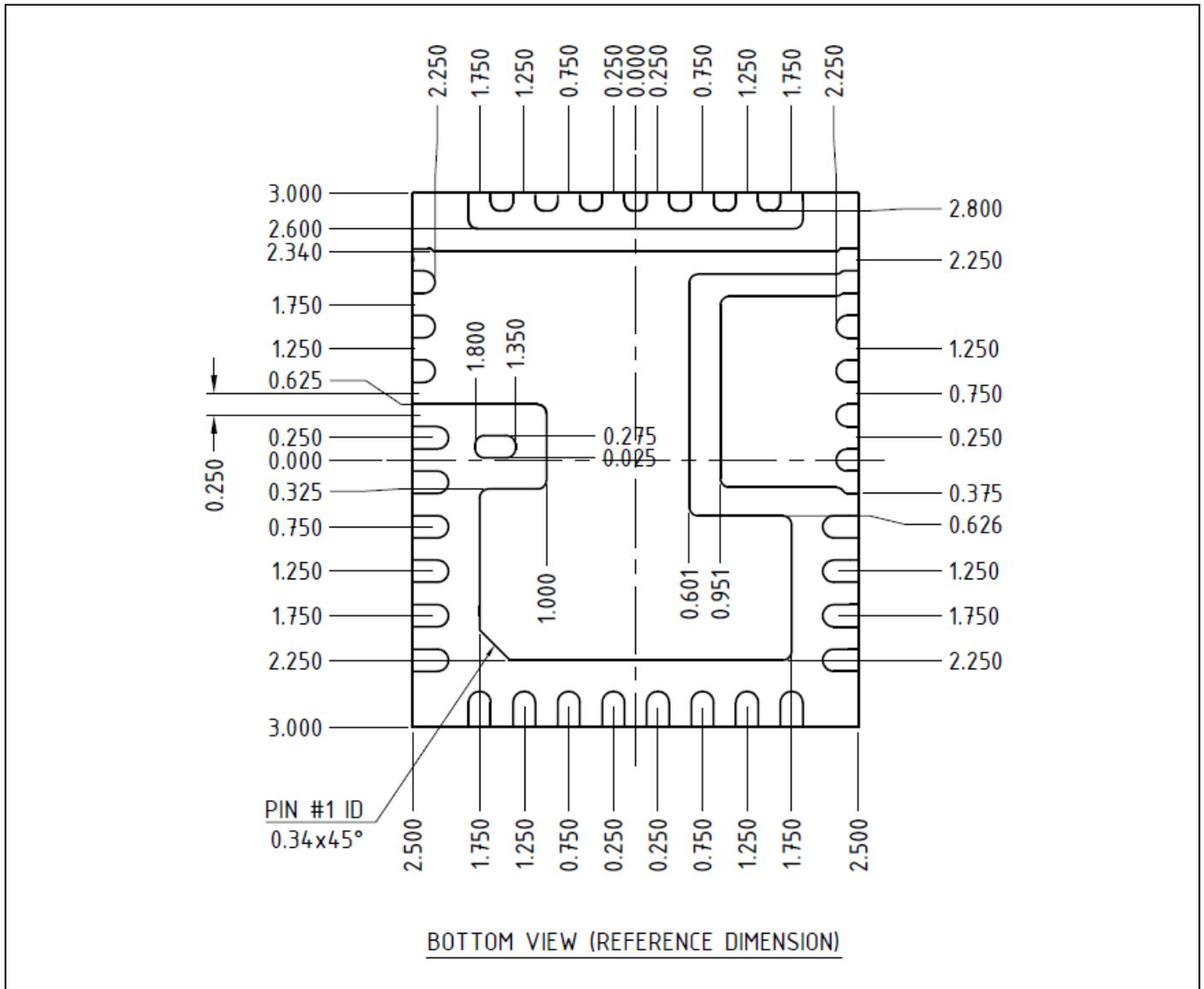
Package

Figure 32   Package Dimensions- Pad Layout

18.3   Tape and Reel Information
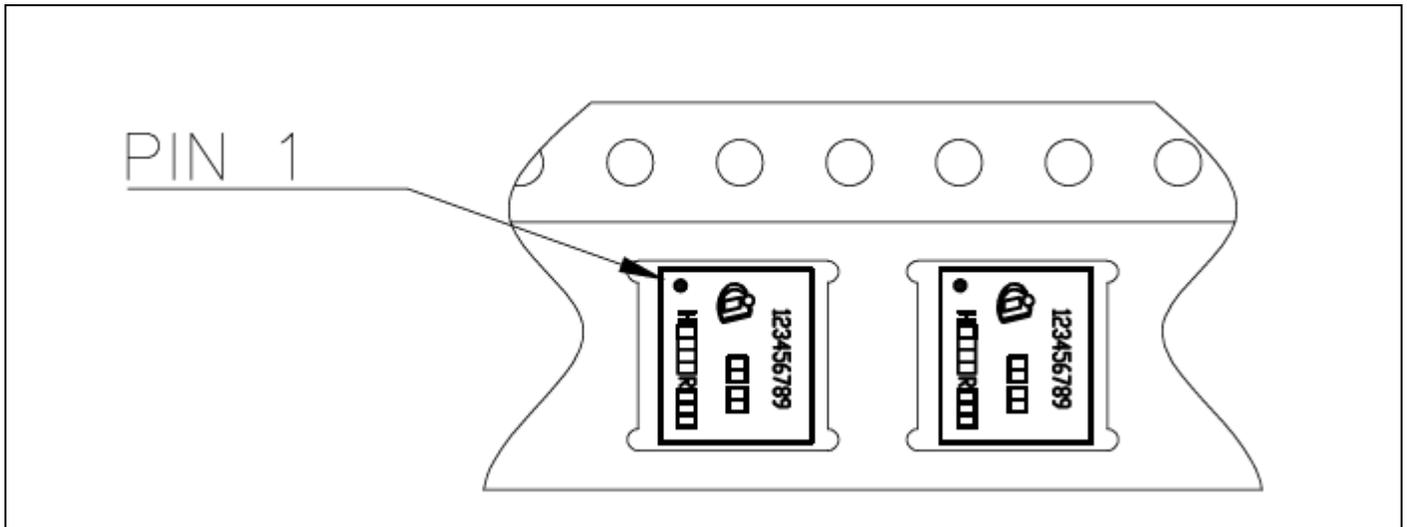
Figure 33   Pin 1 orientation in the Tape & reel

19 Environmental Qualifications

Table 19

Qualification Level	Industrial	
Moisture Sensitivity	5 x 6 mm QFN Package	JEDEC Level 2 @ 260°C
ESD Human Body Model	JESD22-A114F, Class 2 (≥ 2000V to < 4000V)	
Charged Device Model	JESD22-C101-D, Class III (≥ 500V to ≤1000V)	
Machine Model	JESD22-A115A, Class A (<200V)	
RoHS2 Compliant	Yes, with exemption 7a	

20   Revision history

Revision	Date	Description
0.9	01/07/2020	Initial release
1.0	12/07/2020	Preliminary Release
1.1	03/04/2021	Changed the maximum number of USER image writes from 48 to 24
1.7	01/11/2022	Updated the electrical spec Table
1.8	01/24/2022	Updated the block Digram Added the new Application Diagram (Figure 5) Updated the communication pin definition when not being used Updated the Electrical Specs Table

Revision History

TDA38640

Revision: 2022-03-13, Rev. 1.7

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2021-03-18	Release of preliminary version of Rev 2 silicon
1.1	2021-03-22	This is the preliminary version of the C11 datasheet TDA38640
1.2	2021-04-20	The Block Diagram was corrected
1.3	2021-05-12	Updated the revision number of the document and the block diagram of the IC
1.4	2021-06-07	Updated the section on Internal LDO and Enable
1.5	2021-10-12	Updated Electrical Specs Table and PMBUs Commands
1.6	2021-12-13	I updated the absolute maximum rating table
1.7	2022-03-13	I have updated multiple items in the datasheet