TEXAS INSTRUMENTS

TMUX8108, TMUX8109
SCDS435A – SEPTEMBER 2021 – REVISED DECEMBER 2021

TMUX810x 100-V, Flat R$_{ON}$, Single 8:1 and Dual 4:1 Multiplexers with Latch-Up Immunity and 1.8-V Logic

1 Features

- High supply voltage capable:
  - Dual supply: ±10 V to ±50 V
  - Single supply: 10 V to 100 V
  - Asymmetric dual supply operation
- Consistent parametrics across supply voltages
- Latch-up immune
- Low crosstalk: −110 dB
- Low input leakage: 40 pA
- Low on resistance flatness: 0.5 Ω
- Removes need for additional logic rail (V$_L$)
- 1.8 V Logic capable
- Fail-safe logic: up to 48 V independent of supply
- Integrated pull-down resistor on logic pins
- Bidirectional signal path
- Break-before-make switching
- Wide operating temperature T$_A$: –40°C to 125°C
- Industry-standard TSSOP and smaller WQFN packages

2 Applications

- High voltage bidirectional switching
- Analog and digital multiplexing and demultiplexing
- Semiconductor test equipment
- LCD test equipment
- Battery test equipment
- Data acquisition systems (DAQ)
- Digital multi-meter (DMM)
- Factory automation and control
- Programmable logic controllers (PLC)
- Analog input modules

3 Description

The TMUX8108 and TMUX8109 are modern high voltage capable analog multiplexers in 8:1 (single ended) and 4:1 (differential) configurations. The devices work well with dual supplies, a single supply, or asymmetric supplies up to a maximum supply voltage of 100 V. The TMUX810x devices provide consistent analog parametric performance across the entire supply voltage range. The TMUX8108 and TMUX8109 support bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins.

All logic inputs support logic levels of 1.8 V, 3.3 V, 5V and can be connected as high as 48 V, allowing for system flexibility with control signal voltage. Fail-safe logic circuitry allows voltages on the logic pins to be applied before the supply pin, protecting the device from potential damage.
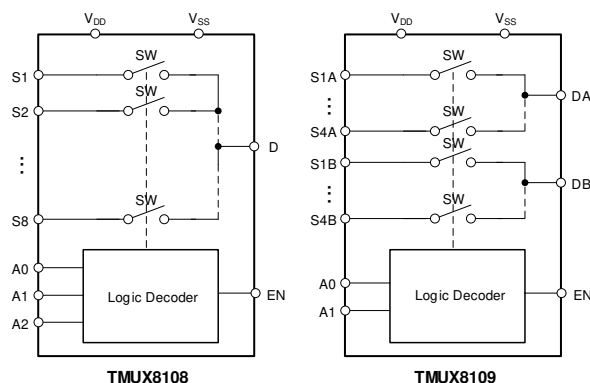
The device family provides latch-up immunity, preventing undesirable high current events between parasitic structures within the device. A latch-up condition typically continues until the power supply rails are turned off and can lead to device failure. The latch-up immunity feature allows this family of multiplexers to be used in harsh environments.

Device Information

PART NUMBER[1]	PACKAGE	BODY SIZE (NOM)
TMUX8108 TMUX8109	TSSOP (16)	5.00 mm × 4.40 mm
	WQFN (16)[2]	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) Preview package.

TMUX8108 and TMUX8109 Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (September 2021) to Revision A (December 2021)	Page
• Changed the status of the data sheet from: *Advanced Information* to: *Production Data*	1

Product Folder Links: *TMUX8108 TMUX8109*

5 Device Comparison Table

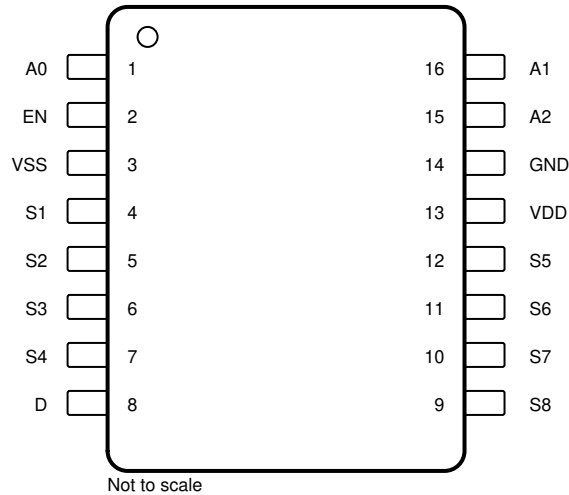| PRODUCT	DESCRIPTION
TMUX8108	Single channel 8:1 multiplexer
TMUX8109	Dual channel 4:1 multiplexer

6 Pin Configuration and Functions

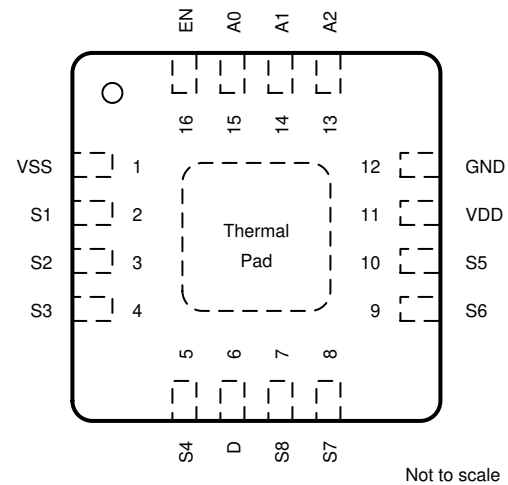**Figure 6-1. PW Package 16-Pin TSSOP Top View**

Figure 6-2. RUM Package 16-Pin WQFN Top View

Table 6-1. Pin Functions: TMUX8108

PIN			TYPE[1]	DESCRIPTION
NAME	TSSOP	WQFN		
A0	1	15	I	Logic control input address 0 (A0).
EN	2	16	I	Active high digital enable (EN) pin. The device is disabled and all switches become high impedance when the pin is low. When the pin is high, the Ax logic inputs determine individual switch states.
V_{SS}	3	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
S1	4	2	I/O	Source pin 1. Can be an input or output.
S2	5	3	I/O	Source pin 2. Can be an input or output.
S3	6	4	I/O	Source pin 3. Can be an input or output.
S4	7	5	I/O	Source pin 4. Can be an input or output.
D	8	6	I/O	Drain pin. Can be an input or output.
S8	9	7	I/O	Source pin 8. Can be an input or output.
S7	10	8	I/O	Source pin 7. Can be an input or output.
S6	11	9	I/O	Source pin 6. Can be an input or output.
S5	12	10	I/O	Source pin 5. Can be an input or output.
V_{DD}	13	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
GND	14	12	P	Ground (0 V) reference
A2	15	13	I	Logic control input address 2 (A2).
A1	16	14	I	Logic control input address 1 (A1).
Thermal Pad		—		The thermal pad is not connected internally. It is recommended that the pad be tied to GND or VSS for the best performance.

(1)   I = input, O = output, I/O = input and output, P = power

Product Folder Links: *TMUX8108 TMUX8109*

Figure 6-3. PW Package 16-Pin TSSOP Top View

Figure 6-4. RUM Package 16-Pin WQFN Top View

Table 6-2. Pin Functions: TMUX8109

PIN			TYPE[1]	DESCRIPTION
NAME	TSSOP	WQFN		
A0	1	15	I	Logic control input address 0 (A0).
EN	2	16	I	Active high digital enable (EN) pin. The device is disabled and all switches become high impedance when the pin is low. When the pin is high, the Ax logic inputs determine individual switch states.
V_{SS}	3	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
S1A	4	2	I/O	Source pin 1A. Can be an input or output.
S2A	5	3	I/O	Source pin 2A. Can be an input or output.
S3A	6	4	I/O	Source pin 3A. Can be an input or output.
S4A	7	5	I/O	Source pin 4A. Can be an input or output.
DA	8	6	I/O	Drain terminal A. Can be an input or output.
DB	9	7	I/O	Drain terminal B. Can be an input or output
S4B	10	8	I/O	Source pin 4B. Can be an input or output.
S3B	11	9	I/O	Source pin 3B. Can be an input or output.
S2B	12	10	I/O	Source pin 2B. Can be an input or output.
S1B	13	11	I/O	Source pin 1B. Can be an input or output.
V_{DD}	14	12	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
GND	15	13	P	Ground (0 V) reference
A1	16	14	I	Logic control input address 1 (A1).
Thermal Pad		—		The thermal pad is not connected internally. It is recommended that the pad be tied to GND or VSS for the best performance.

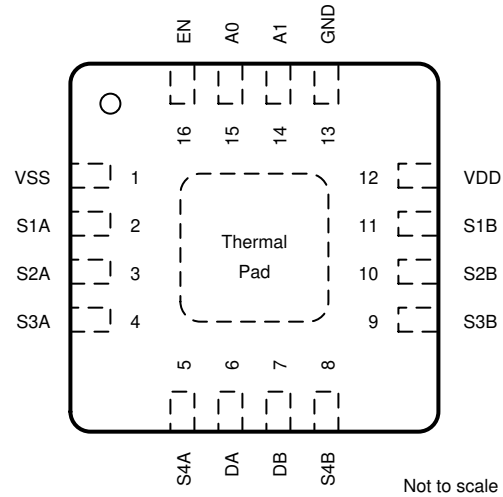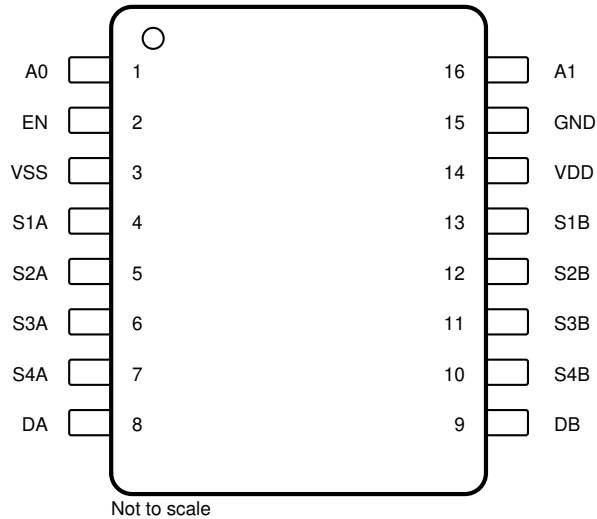(1)   I = input, O = output, I/O = input and output, P = power

7 Specifications

7.1 Absolute Maximum Ratings: TMUX810x Devices

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{DD}–V_{SS}			110	V
V_{DD}	Supply voltage	−0.5	110	V
V_{SS}		−110	0.5	V
V_{Ax} or V_{EN}	Logic control input pin voltage (Ax, EN)	−0.5	50	V
I_{Ax} or I_{EN}	Logic control input pin current (Ax, EN)	−30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)	V_{SS}−2	V_{DD}+2	V
$I_{DC\ (CONT)}$	Source or drain continuous current (Sx, D)	−100	100	mA
I_{IK} [2]	Diode clamp current at 85°C	−100	100	mA
	Diode clamp current at 125°C	−15	15	mA
T_{stg}	Storage temperature	−65	150	°C
T_A	Ambient temperature	−55	150	°C
T_J	Junction temperature		150	°C
P_{tot} [3]	Total power dissipation (TSSOP)		720	mW

(1)   Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2)   Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.

(3)   For TSSOP package: P_{tot} derates linearly above T_A = 70°C by 10.5 mW/°C

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins[2]	±500	

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Product Folder Links: *TMUX8108 TMUX8109*

7.3 Recommended Operating Conditions: TMUX810x Devices

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{DD} - V_{SS}$ [(1)]	Power supply voltage differential		10		100	V
V_{DD}	Positive power supply voltage		10		100	V
V_S or V_D [(2)]	Signal path input/output voltage (source or drain pin)		V_{SS}		V_{DD}	V
V_A or V_{EN}	Address or enable pin voltage		0		48	V
T_A	Ambient temperature		–40		125	°C
V_S or V_D [(2)]	Signal path input/output voltage (source or drain pin)		V_{SS}		V_{DD}	V
T_A	Ambient temperature		–40		125	°C
I_{DC} 1ch.[(3)]	Continuous current through switch for TSSOP or QFN on 1 channel				100	mA
I_{DC} All ch.[(4)]	Continuous current through switch on all channels at the same time, TSSOP package	T_A = 25°C			75	mA
		T_A = 85°C			50	mA
		T_A = 125°C			25	mA

(1) V_{DD} and V_{SS} can be any value as long as 10 V ≤ (V_{DD} – V_{SS}) ≤ 100 V, and the minimum V_{DD} is met.
(2) V_S or V_D is the voltage on any Source or Drain pins.
(3)   Max continuous current shown for a single channel at a time.
(4)   Max continuous current shown for all channels at a time. Refer to max power dissipation (P_{tot}) to ensure package limitations are not violated.

7.4 Thermal Information

THERMAL METRIC[(1)]		TMUX8108	TMUX8109	UNIT
		PW (TSSOP)	PW (TSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97.0	96.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.7	26.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.8	43.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.1	1.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.1	42.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1)   For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics (Global): TMUX810x Devices

over operating free-air temperature range (unless otherwise noted)
typical at V_{DD} = +36 V, V_{SS} = –36 V, GND = 0 V and T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
LOGIC INPUTS							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		48	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current	Logic inputs = 0 V, 5 V, or 48 V	–40°C to +125°C		0.4	3.8	µA
I_{IL}	Input leakage current	Logic inputs = 0 V, 5 V, or 48 V	–40°C to +125°C	–0.2	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic inputs = 0 V, 5 V, or 48 V	25°C		250	500	µA
			–40°C to +85°C			500	µA
			–40°C to +125°C			500	µA
I_{SS}	V_{SS} supply current	Logic inputs = 0 V, 5 V, or 48 V	25°C		250	420	µA
			–40°C to +85°C			420	µA
			–40°C to +125°C			420	µA

7.6 Electrical Characteristics (±15-V Dual Supply)

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, GND = 0 V (unless otherwise noted)
Typical at T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –5 mA	25°C		38	55	Ω
			–40°C to +85°C			75	
			–40°C to +125°C			90	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –5 mA	25°C		0.65		Ω
			–40°C to +85°C			1.5	
			–40°C to +125°C			2.1	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10 V to +10 V I_D = –5 mA	25°C		0.5		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –5 mA	–40°C to +125°C		0.25		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / +10 V	25°C		0.01		nA
			–40°C to +85°C	–3		3	
			–40°C to +125°C	–15		15	
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / +10 V	25°C		0.04		nA
			–40°C to +85°C	–8		8	
			–40°C to +125°C	–40		40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V	25°C		0.04		nA
			–40°C to +85°C	–8		8	
			–40°C to +125°C	–40		40	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels[2]	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V	25°C		5		pA
			85°C		50		
			125°C		900		

(1) When V_S is positive, V_D is negative. And when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. And when V_D is at a voltage potential, V_S is floating.

7.7 Electrical Characteristics (±36-V Dual Supply)

V_{DD} = +36 V ± 10%, V_{SS} = –36 V ± 10%, GND = 0 V (unless otherwise noted)
Typical at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = -25 V to +25 V I_D = –5 mA	25°C		38	48	Ω
			–40°C to +85°C			65	
			–40°C to +125°C			80	
ΔR_{ON}	On-resistance mismatch between channels	V_S = -25 V to +25 V I_D = –5 mA	25°C		0.65		Ω
			–40°C to +85°C			1.5	
			–40°C to +125°C			2.1	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = -25 V to +25 V I_D = –5 mA	25°C		0.9		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –5 mA	–40°C to +125°C		0.25		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 39.6 V, V_{SS} = –39.6 V Switch state is off V_S = +25 V / –25 V V_D = –25 V / +25 V	25°C		0.01		nA
			–40°C to +85°C	–3		3	
			–40°C to +125°C	–15		15	
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 39.6 V, V_{SS} = –39.6 V Switch state is off V_S = +25 V / –25 V V_D = –25 V / +25 V	25°C		0.06		nA
			–40°C to +85°C	–8		8	
			–40°C to +125°C	–40		40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 39.6 V, V_{SS} = –39.6 V Switch state is on $V_S = V_D$ = ±25 V	25°C		0.06		nA
			–40°C to +85°C	–8		8	
			–40°C to +125°C	–40		40	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels[2]	V_{DD} = 39.6 V, V_{SS} = –39.6 V Switch state is on $V_S = V_D$ = ±25 V	25°C		5		pA
			85°C		30		
			125°C		100		

(1)   When V_S is positive, V_D is negative. And when V_S is negative, V_D is positive.
(2)   When V_S is at a voltage potential, V_D is floating. And when V_D is at a voltage potential, V_S is floating.

Product Folder Links: *TMUX8108 TMUX8109*

7.8 Electrical Characteristics (±50-V Dual Supply)

V_{DD} = +50 V, V_{SS} = –50 V, GND = 0 V (unless otherwise noted)
Typical at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –45 V to +45 V I_D = –5 mA	25°C		38	48	Ω
			–40°C to +85°C			65	
			–40°C to +125°C			80	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –45 V to +45 V I_D = –5 mA	25°C		0.65		Ω
			–40°C to +85°C			1.5	
			–40°C to +125°C			2.1	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –45 V to +45 V I_D = –5 mA	25°C		1		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –5 mA	–40°C to +125°C		0.25		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 50 V, V_{SS} = –50 V Switch state is off V_S = +45 V / –45 V V_D = –45 V / +45 V	25°C		0.02		nA
			–40°C to +85°C	–3		3	
			–40°C to +125°C	–15		15	
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 50 V, V_{SS} = –50 V Switch state is off V_S = +45 V / –45 V V_D = –45 V / +45 V	25°C		0.09		nA
			–40°C to +85°C	–8		8	
			–40°C to +125°C	–40		40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 50 V, V_{SS} = –50 V Switch state is on V_S = V_D = ±45 V	25°C		0.09		nA
			–40°C to +85°C	–8		8	
			–40°C to +125°C	–40		40	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels[2]	V_{DD} = 50 V, V_{SS} = –50 V Switch state is on V_S = V_D = ±45 V	25°C		10		pA
			85°C		40		
			125°C		170		

(1) When V_S is positive, V_D is negative. And when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating. And when V_D is at a voltage potential, V_S is floating.

7.9 Electrical Characteristics (72-V Single Supply)

V_{DD} = +72 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to +60 V I_D = –5 mA	25°C		38	48	Ω
			–40°C to +85°C			65	
			–40°C to +125°C			80	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to +60 V I_D = –5 mA	25°C		0.65		Ω
			–40°C to +85°C			1.5	
			–40°C to +125°C			2.1	
$R_{ON FLAT}$	On-resistance flatness	V_S = 0 V to +60 V I_D = –5 mA	25°C		0.6		Ω
$R_{ON DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –5 mA	–40°C to +125°C		0.25		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	Switch state is off V_S = +60 V / 1 V V_D = 1 V / +60 V	25°C		0.02		nA
			–40°C to +85°C	–3		3	
			–40°C to +125°C	–15		15	
$I_{D(OFF)}$	Drain off leakage current[1]	Switch state is off V_S = +60 V / 1 V V_D = 1 V / +60 V	25°C		0.06		nA
			–40°C to +85°C	–8		8	
			–40°C to +125°C	–40		40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	Switch state is on V_S = V_D = 1 V / +60 V	25°C		0.07		nA
			–40°C to +85°C	–8		8	
			–40°C to +125°C	–40		40	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels[2]	Switch state is on V_S = V_D = 1 V / +60 V	25°C		20		pA
			85°C		50		
			125°C		120		

(1)   When V_S is 60 V, V_D is 1 V. Or when V_S is 1 V, V_D is 60 V.
(2)   When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

Product Folder Links: *TMUX8108 TMUX8109*

7.10 Electrical Characteristics (100-V Single Supply)

V_{DD} = +100 V, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to +95 V I_D = –5 mA	25°C		38	48	Ω
			–40°C to +85°C			65	
			–40°C to +125°C			80	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to +95 V I_D = –5 mA	25°C		0.65		Ω
			–40°C to +85°C			1.5	
			–40°C to +125°C			2.1	
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to +95 V I_D = –5 mA	25°C		0.6		Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –5 mA	–40°C to +125°C		0.25		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	Switch state is off V_S = +95 V / 1 V V_D = 1 V / +95 V	25°C		0.02		nA
			–40°C to +85°C	–3		3	
			–40°C to +125°C	–15		15	
$I_{D(OFF)}$	Drain off leakage current[1]	Switch state is off V_S = +95 V / 1 V V_D = 1 V / +95 V	25°C		0.09		nA
			–40°C to +85°C	–8		8	
			–40°C to +125°C	–40		40	
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	Switch state is on V_S = V_D = 1 V / +95 V	25°C		0.1		nA
			–40°C to +85°C	–8		8	
			–40°C to +125°C	–40		40	
$\Delta I_{S(ON)}$ $\Delta I_{D(ON)}$	Leakage current mismatch between channels[2]	Switch state is on V_S = V_D = 1 V / +95 V	25°C		50		pA
			85°C		120		
			125°C		350		

(1) When V_S is 95 V, V_D is 1 V. Or when V_S is 1 V, V_D is 95 V.
(2) When V_S is at a voltage potential, V_D is floating. Or when V_D is at a voltage potential, V_S is floating.

7.11 Switching Characteristics: TMUX810x Devices

over operating free-air temperature range (unless otherwise noted)

typical at V_{DD} = +36 V, V_{SS} = –36 V, GND = 0 V and T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 10 V R_L = 10 kΩ, C_L = 15 pF	25°C		3		μs
			–40°C to +85°C			10	
			–40°C to +125°C			12	
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 10 V R_L = 10 kΩ, C_L = 15 pF	25°C		3		μs
			–40°C to +85°C			14	
			–40°C to +125°C			15	
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 10 V R_L = 10 kΩ, C_L = 15 pF	25°C		0.65		μs
			–40°C to +85°C			3	
			–40°C to +125°C			3	
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 10 kΩ, C_L = 15 pF	25°C		3		μs
			–40°C to +85°C	0.1			
			–40°C to +125°C	0.1			
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} ramp rate = 1 V/μs, V_S = 10 V, R_L = 10 kΩ, C_L = 15pF	25°C		75		μs
t_{PD}	Propagation delay	R_L = 50 Ω , C_L = 5 pF	25°C		550		ps
Q_{INJ}	Charge injection	V_S = (V_{DD} + V_{SS}) / 2, C_L = 1 nF	25°C		–150		pC
O_{ISO}	Off isolation	R_L = 50 Ω , C_L = 5 pF V_S = (V_{DD} + V_{SS}) / 2, f = 1 MHz	25°C		–110		dB
X_{TALK}	Crosstalk	R_L = 50 Ω , C_L = 5 pF V_S = (V_{DD} + V_{SS}) / 2, f = 1MHz	25°C		–110		dB
BW	–3dB bandwidth (TMUX8108)	R_L = 50 Ω , C_L = 5 pF V_S = (V_{DD} + V_{SS}) / 2	25°C		200		MHz
BW	–3dB bandwidth (TMUX8109)				380		
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF V_S = (V_{DD} + V_{SS}) / 2, f = 1 MHz	25°C		–2.8		dB
THD+N	Total harmonic distortion + Noise	Dual supply voltage V_{PP} = 5 V, V_{BIAS} = (V_{DD} + V_{SS}) / 2 R_L = 1 kΩ , C_L = 5 pF, f = 20 Hz to 20 kHz	25°C		0.003		%
$C_{S(OFF)}$	Source off capacitance	V_S = (V_{DD} + V_{SS}) / 2, f = 1 MHz	25°C		3		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX8108)	V_S = (V_{DD} + V_{SS}) / 2, f = 1 MHz	25°C		20		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX8109)	V_S = (V_{DD} + V_{SS}) / 2, f = 1 MHz	25°C		10		pF
$C_{S(ON)}, C_{D(ON)}$	On capacitance (TMUX8108)	V_S = (V_{DD} + V_{SS}) / 2, f = 1 MHz	25°C		21		pF
$C_{S(ON)}, C_{D(ON)}$	On capacitance (TMUX8109)	V_S = (V_{DD} + V_{SS}) / 2, f = 1 MHz	25°C		12		pF

7.12 Typical Characteristics

at T_A = 25°C, V_{DD} = +36 V, and V_{SS} = –36 V (unless otherwise noted)

V_{DD} = 36 V, V_{SS} = –36 V

Flatest Ron Region
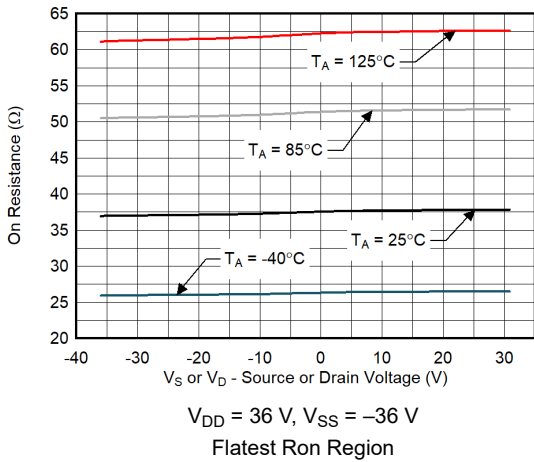
Figure 7-1. On-Resistance vs Source or Drain Voltage

V_{DD} = 36 V, V_{SS} = –36 V
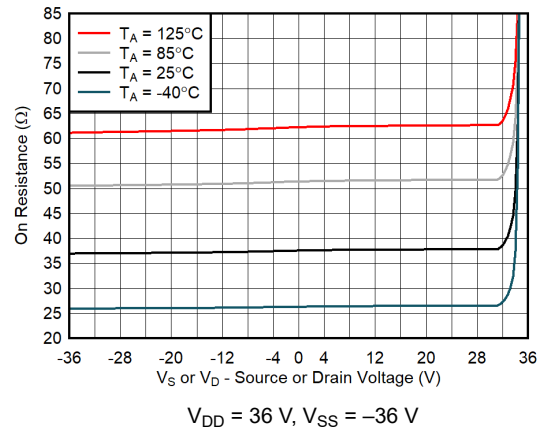
Figure 7-2. On-Resistance vs Source or Drain Voltage

V_{DD} = 36 V, V_{SS} = –36 V
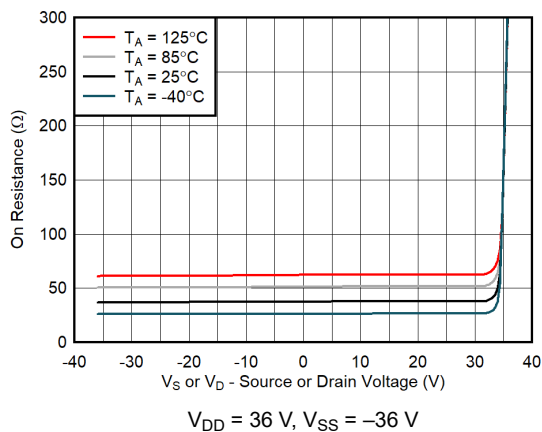
Figure 7-3. On-Resistance vs Source or Drain Voltage

Dual Supply Voltages
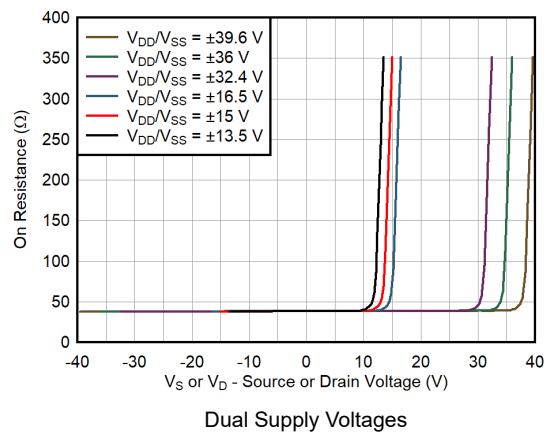
Figure 7-4. On-Resistance vs Source or Drain Voltage

V_{DD} = 15 V, V_{SS} = –15 V
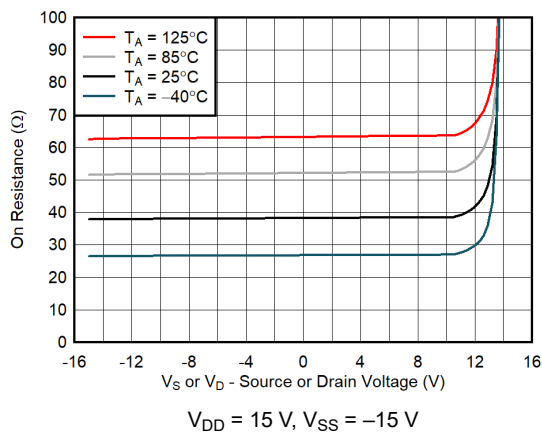
Figure 7-5. On-Resistance vs Source or Drain Voltage

V_{DD} = 15 V, V_{SS} = –15 V
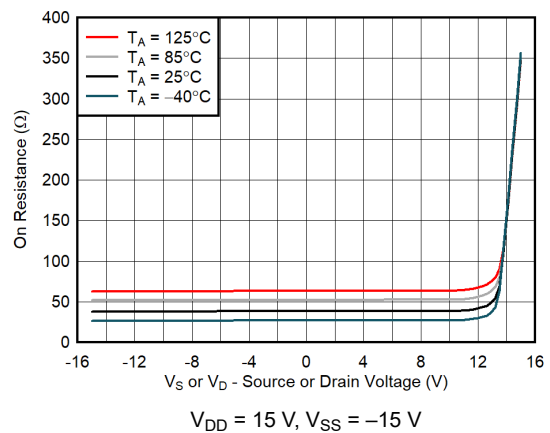
Figure 7-6. On-Resistance vs Source or Drain Voltage

7.12 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = +36 V, and V_{SS} = –36 V (unless otherwise noted)

V_{DD} = 72 V, V_{SS} = 0 V

Figure 7-7. On-Resistance vs Source or Drain Voltage

V_{DD} = 72 V, V_{SS} = 0 V
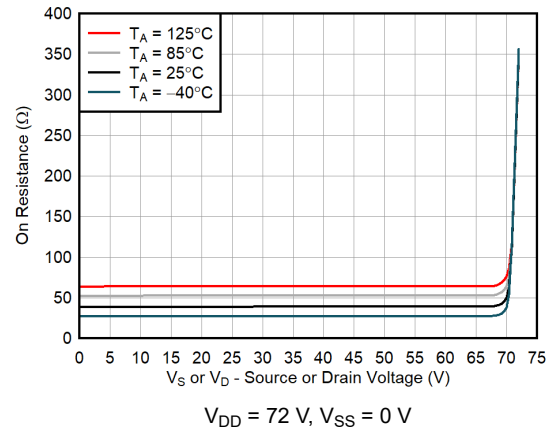
Figure 7-8. On-Resistance vs Source or Drain Voltage

V_{DD} = 100 V, V_{SS} = 0 V
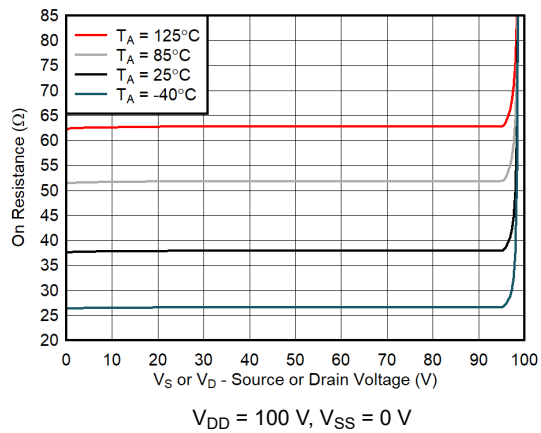
Figure 7-9. On-Resistance vs Source or Drain Voltage

V_{DD} = 100 V, V_{SS} = 0 V
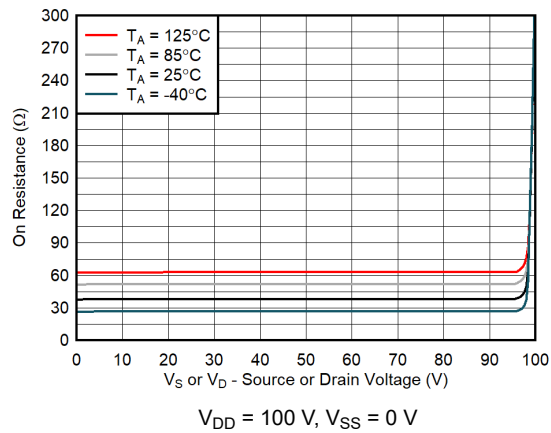
Figure 7-10. On-Resistance vs Source or Drain Voltage

V_{DD} = 36 V, V_{SS} = –36 V
TMUX8108
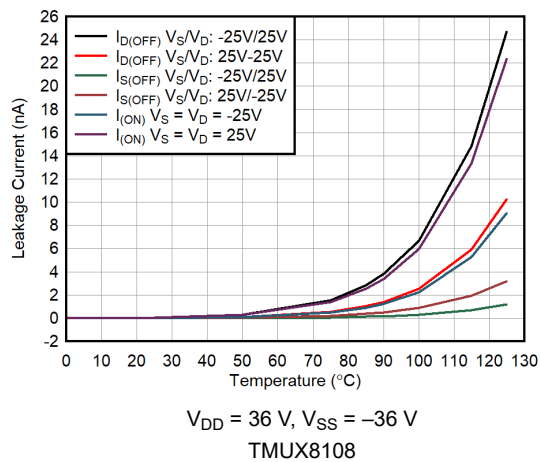
Figure 7-11. Leakage Current vs Temperature

V_{DD} = 36 V, V_{SS} = –36 V
TMUX8109

Figure 7-12. Leakage Current vs Temperature

Product Folder Links: *TMUX8108 TMUX8109*

7.12 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = +36 V, and V_{SS} = –36 V (unless otherwise noted)

V_{DD} = 36 V, V_{SS} = –36 V
TMUX8108

Figure 7-13. Leakage Current vs Temperature

V_{DD} = 36 V, V_{SS} = –36 V
TMUX8109

Figure 7-14. Leakage Current vs Temperature
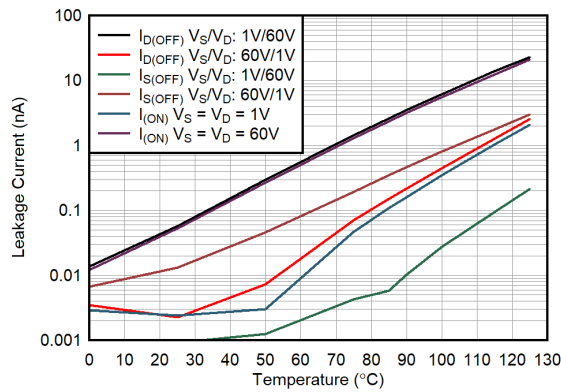
V_{DD} = 72 V, V_{SS} = 0 V
TMUX8108

Figure 7-15. Leakage Current vs Temperature
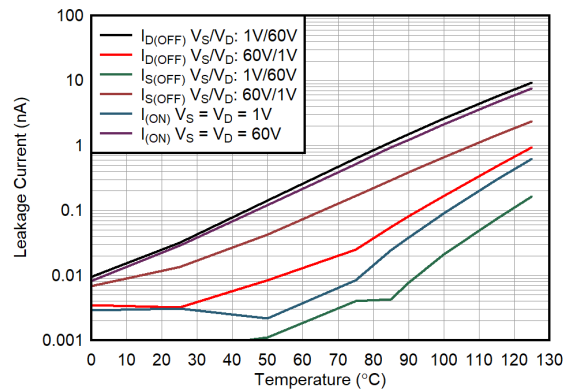
V_{DD} = 72 V, V_{SS} = 0 V
TMUX8109

Figure 7-16. Leakage Current vs Temperature
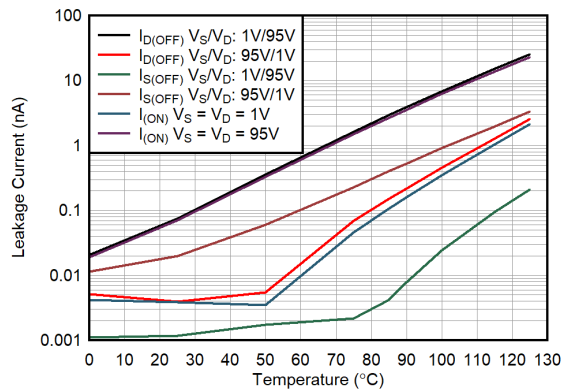
V_{DD} = 100 V, V_{SS} = 0 V
TMUX8108

Figure 7-17. Leakage Current vs Temperature
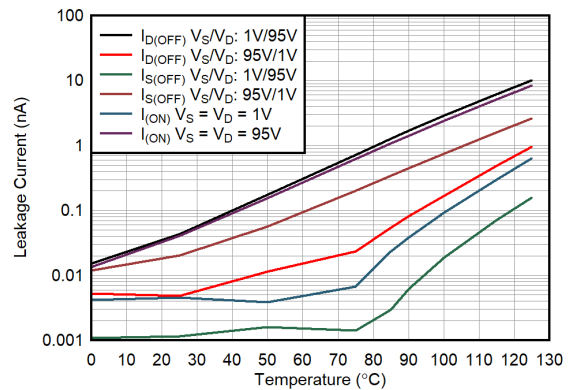
V_{DD} = 100 V, V_{SS} = 0 V
TMUX8109

Figure 7-18. Leakage Current vs Temperature

7.12 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = +36 V, and V_{SS} = –36 V (unless otherwise noted)
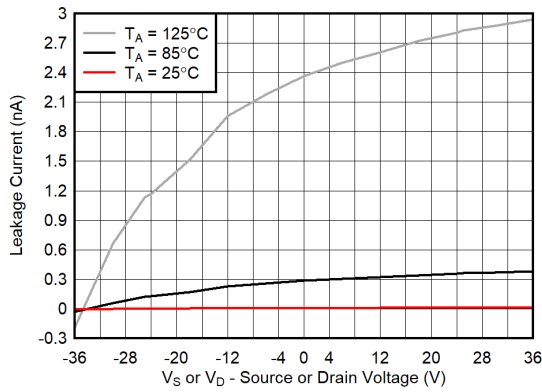
V_{DD} = 36 V, V_{SS} = –36 V
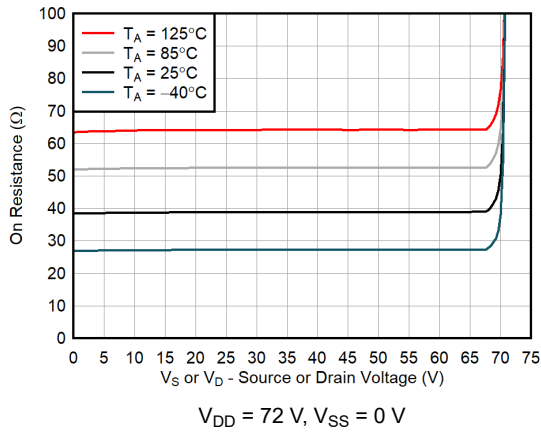TMUX8109 and TMUX8109

Figure 7-19. $I_{S(OFF)}$ Leakage Current vs Source or Drain Voltage
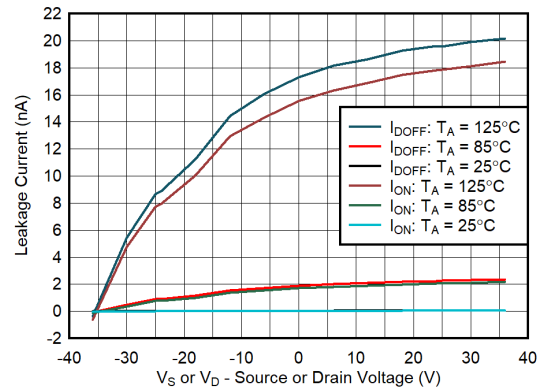
V_{DD} = 36 V, V_{SS} = –36 V
TMUX8108

Figure 7-20. Leakage Current vs Source or Drain Voltage
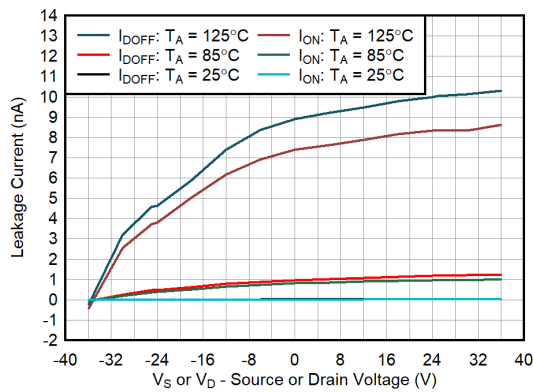
V_{DD} = 36 V, V_{SS} = –36 V
TMUX8109

Figure 7-21. Leakage Current vs Source or Drain Voltage
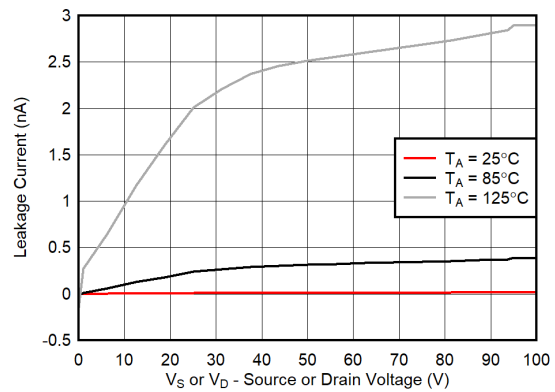
V_{DD} = 100 V, V_{SS} = 0 V
TMUX8108 and TMUX8109

Figure 7-22. $I_{S(OFF)}$ Leakage Current vs Source or Drain Voltage
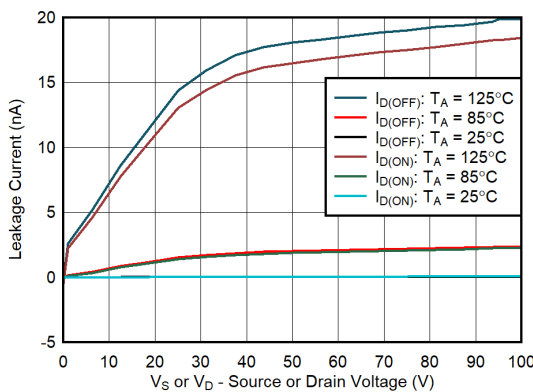
V_{DD} = 100 V, V_{SS} = 0 V
TMUX8108

Figure 7-23. Leakage Current vs Source or Drain Voltage
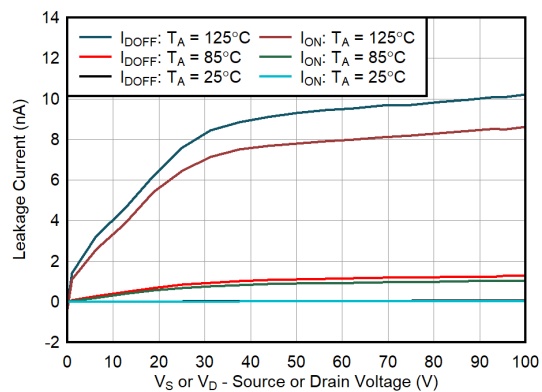
V_{DD} = 100 V, V_{SS} = 0 V
TMUX8109

Figure 7-24. Leakage Current vs Source or Drain Voltage

Product Folder Links: *TMUX8108 TMUX8109*

7.12 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = +36 V, and V_{SS} = –36 V (unless otherwise noted)
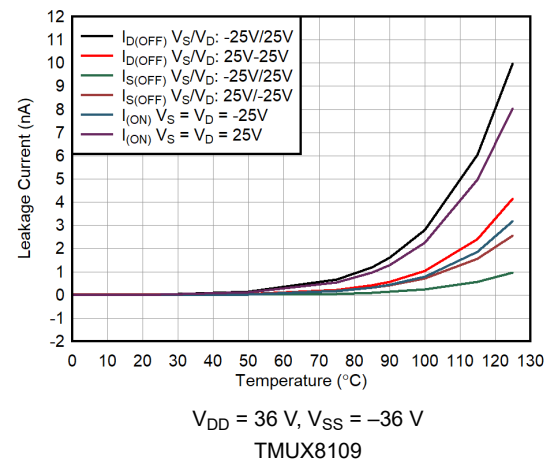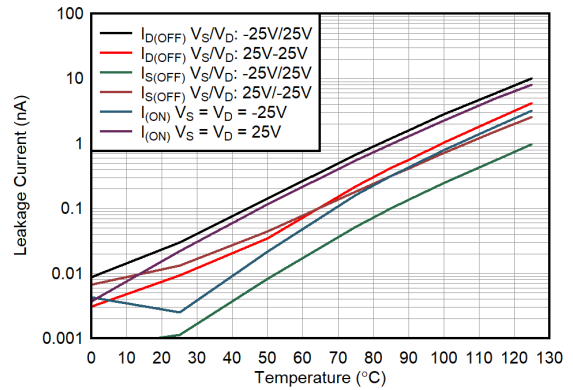

V_{DD} = 36 V, V_{SS} = –36 V

Figure 7-25. Charge Injection vs Source Voltage
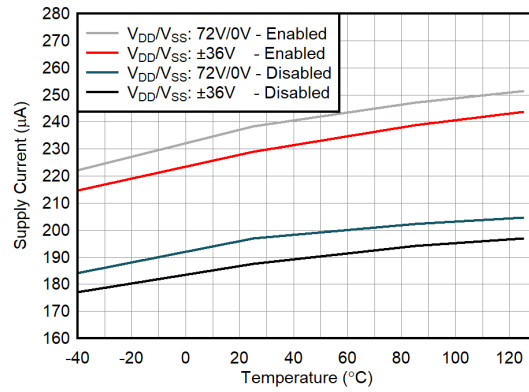
Figure 7-26. Supply Current vs Temperature

V_{DD} = 36 V, V_{SS} = –36 V
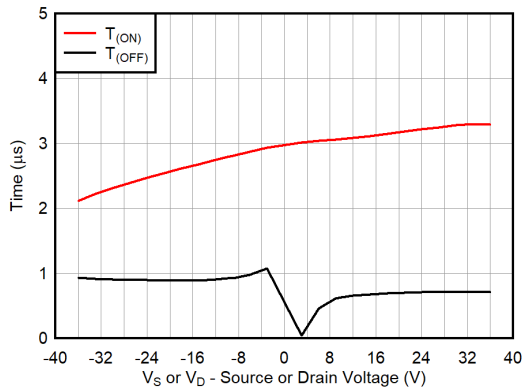
Figure 7-27. Turn-On and Turn-Off Times vs Source Voltage

T_A = 25°C
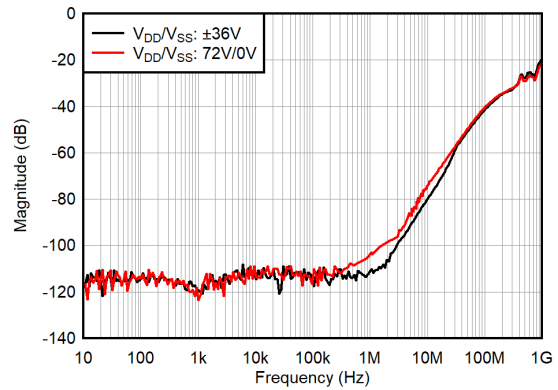
Figure 7-28. Off Isolation vs Frequency

T_A = 25°C
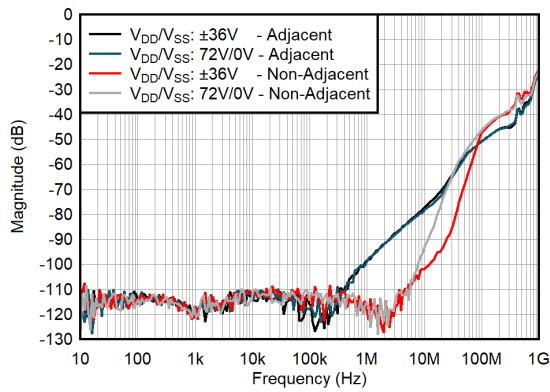
Figure 7-29. Crosstalk vs Frequency

Bandwidth
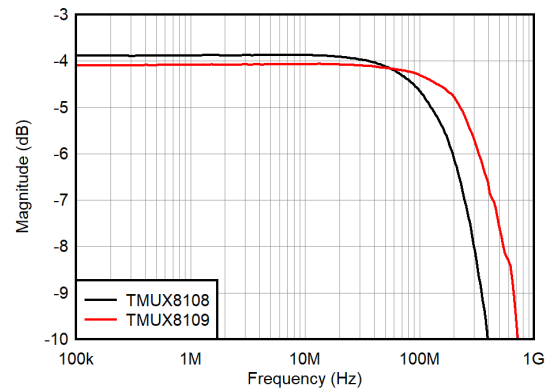
Figure 7-30. Insertion Loss vs Frequency

Product Folder Links: *TMUX8108 TMUX8109*

8 Parameter Measurement Information

8.1 On-Resistance

The on-resistance of the TMUX8108 and TMUX8109 is the ohmic resistance across the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. Figure 8-1 shows how the symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in . ΔR_{ON} represents the difference between the R_{ON} of any two channels, while R_{ON_FLAT} denotes the flatness that is defined as the difference between the maximum and minimum value of on-resistance measured over the specified analog signal range.

$$R_{ON} = \frac{V}{I_S}$$
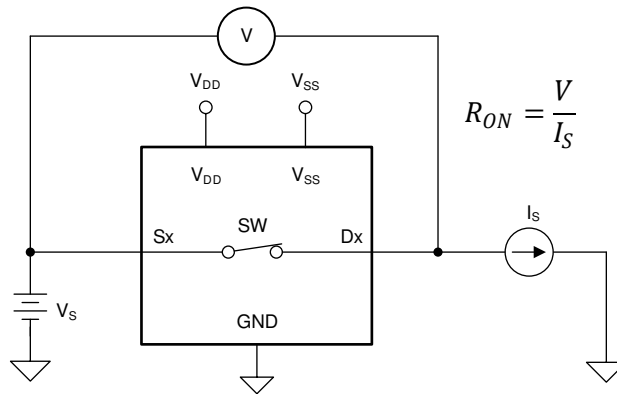
Figure 8-1. On-Resistance Measurement Setup

8.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current $I_{S(OFF)}$: the leakage current flowing into or out of the source pin when the switch is off.
2. Drain off-leakage current $I_{D(OFF)}$: the leakage current flowing into or out of the drain pin when the switch is off.

Figure 8-2 shows the setup used to measure both off-leakage currents.
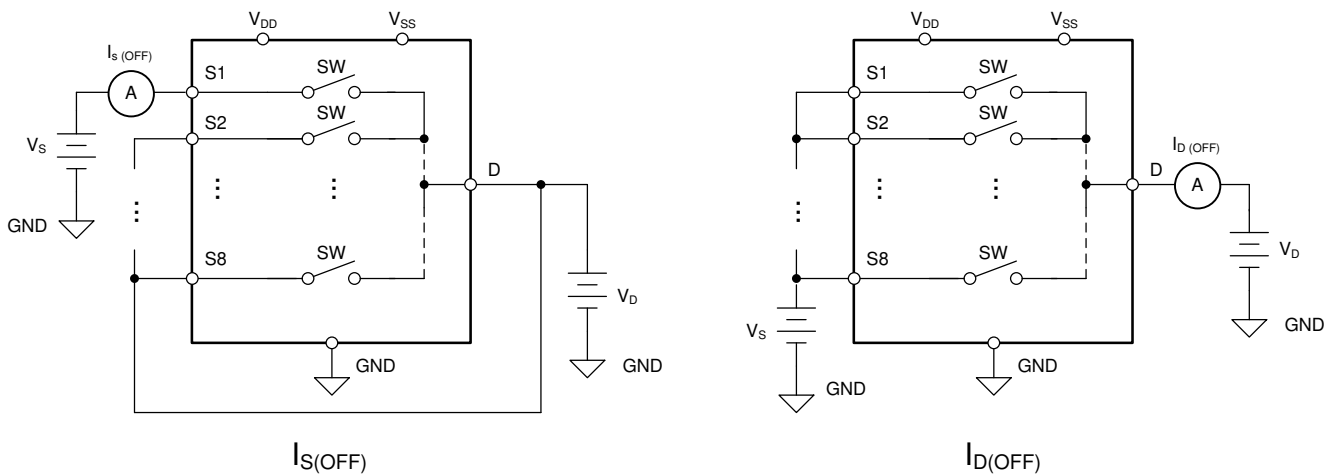
Figure 8-2. Off-Leakage Measurement Setup

Product Folder Links: TMUX8108 TMUX8109

8.3 On-Leakage Current

Source on-leakage current ($I_{S(ON)}$) and drain on-leakage current ($I_{D(ON)}$) denote the channel leakage currents when the switch is in the on state. $I_{S(ON)}$ is measured with the drain floating, while $I_{D(ON)}$ is measured with the source floating. Figure 8-3 shows the circuit used for measuring the on-leakage currents.
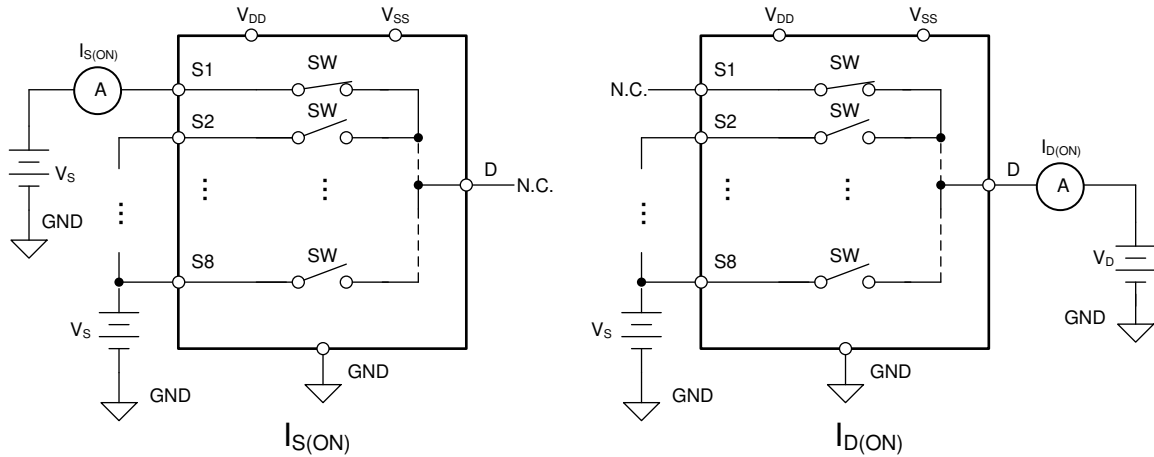
Figure 8-3. On-Leakage Measurement Setup

8.4 Break-Before-Make Delay

The break-before-make delay is a safety feature of the TMUX8108 and TMUX8109. The ON switches first break the connection before the OFF switches make connection. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 8-4 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.
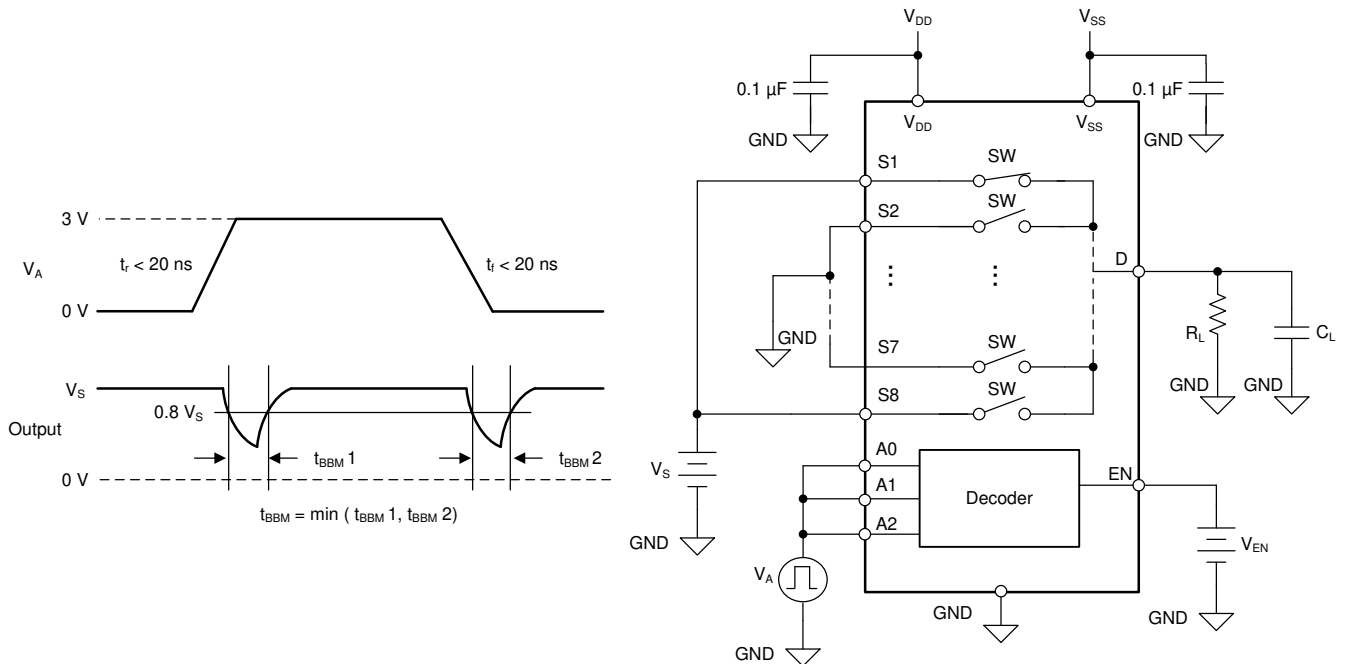
Figure 8-4. Break-Before-Make Delay Measurement Setup

Product Folder Links: *TMUX8108 TMUX8109*

8.5 Enable Turn-on and Turn-off Time

$t_{ON(EN)}$ time is defined as the time taken by the output of the TMUX8108 and TMUX8109 to rise to a 90% final value after the EN signal has risen to a 50% final value. $t_{OFF(EN)}$ is defined as the time taken by the output of the TMUX8108 and TMUX8109 to fall to a 10% final value after the EN signal has fallen to a 50% initial value. Figure 8-5 shows the setup used to measure the enable delay time.
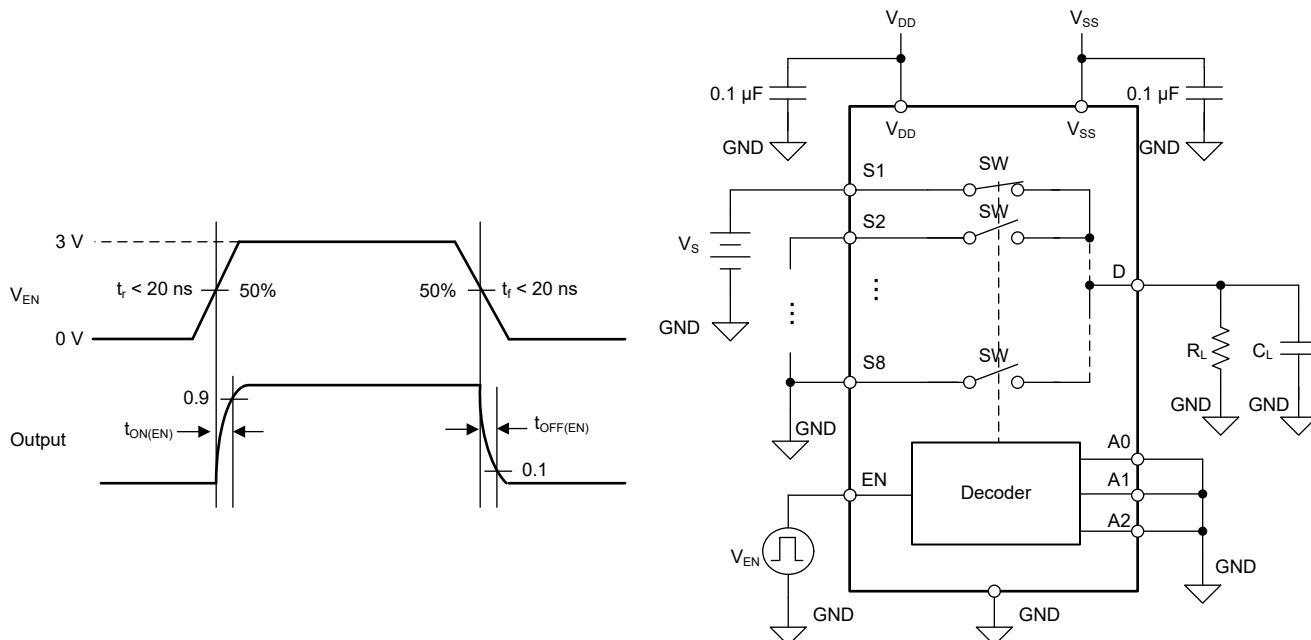
Figure 8-5. Enable Delay Measurement Setup

8.6 Transition Time

Transition time is defined as the time taken by the output of the device to rise (to 90% of the transition) or fall (to 10% of the transition) after the address signal (Ax) has fallen or risen to 50% of the transition. Figure 8-6 shows the setup used to measure transition time, denoted by the symbol t_{TRAN}.
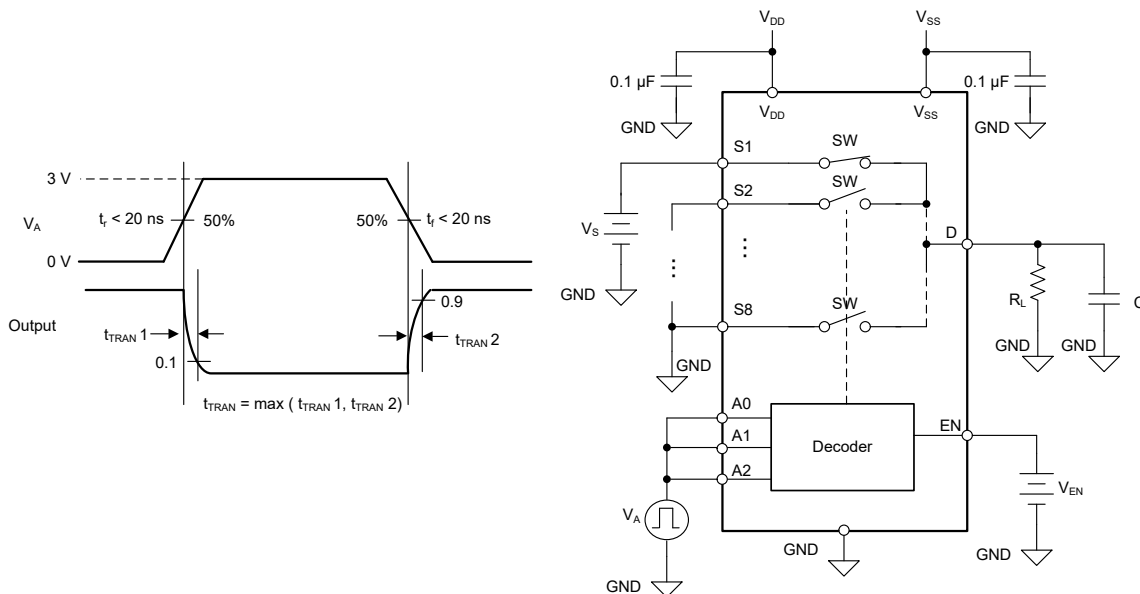
Figure 8-6. Transition Time Measurement Setup

Product Folder Links: *TMUX8108 TMUX8109*

8.7 Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching, and is denoted by the symbol Q_{INJ}. Figure 8-7 shows the setup used to measure charge injection from the source to drain.
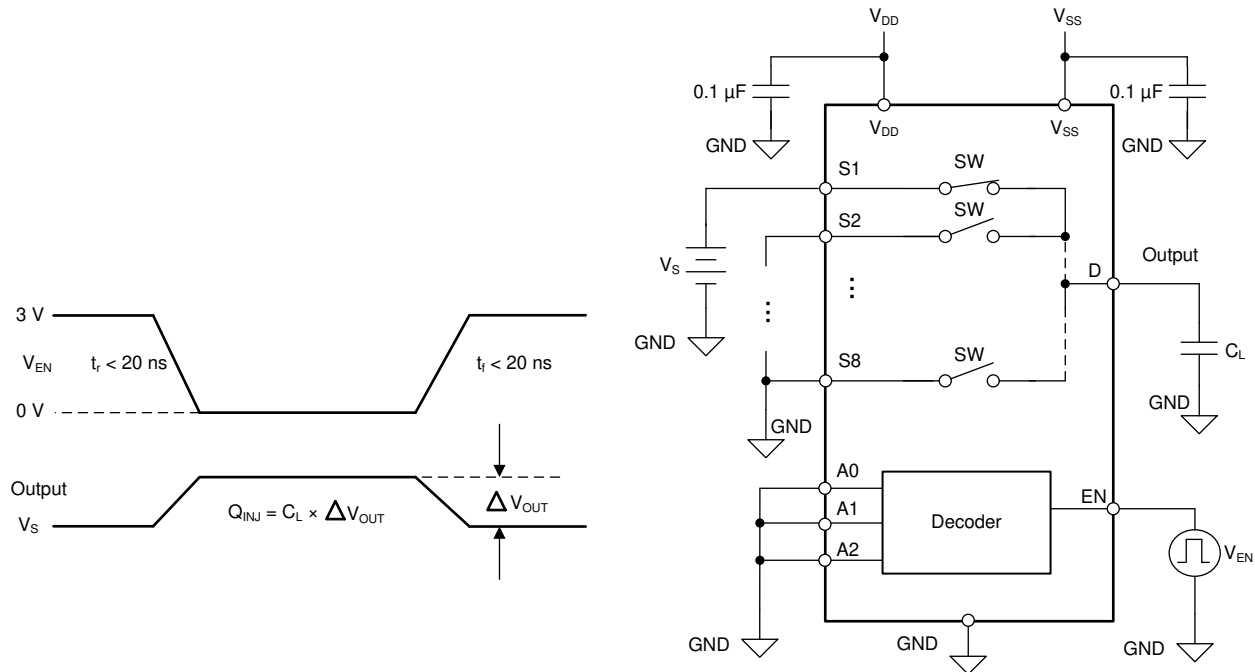
Figure 8-7. Charge-Injection Measurement Setup

8.8 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance for the measurement (Z_O) is 50 Ω. Figure 8-8 shows the setup used to measure off isolation.

$$Off\ Isolation = 20 \times Log\frac{V_{OUT}}{V_S}$$
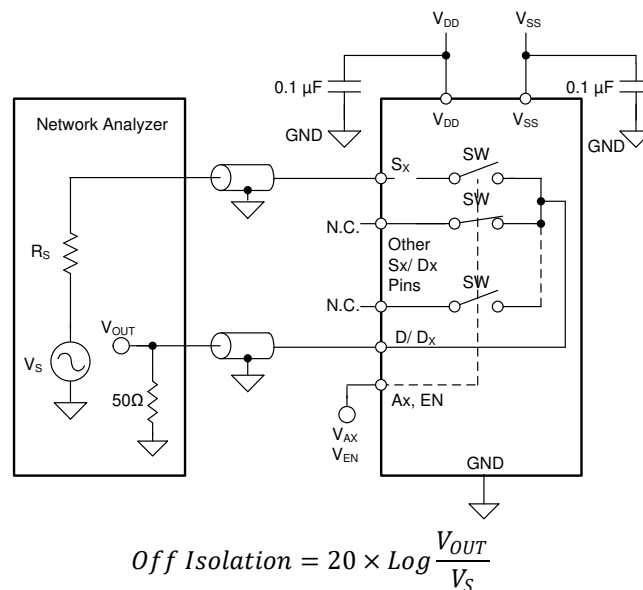
Figure 8-8. Off Isolation Measurement Setup

8.9 Crosstalk

There are two types of crosstalk that can be defined for the devices:

1. Intra-channel crosstalk ($X_{TALK(INTRA)}$): the voltage at the source pin (Sx) of an off-switch input when a signal is applied at the source pin of an on-switch input in the same channel, as shown in Figure 8-9 .
2. Inter-channel crosstalk ($X_{TALK(INTER)}$): the voltage at the source pin (Sx) of an on-switch input when a signal is applied at the source pin of an on-switch input in a different channel, as shown in Figure 8-10. Inter-channel crosstalk applies only to the TMUX8109 device.

$$Intra - channel\ Crosstalk = 20 \times Log\frac{V_{OUT}}{V_S}$$
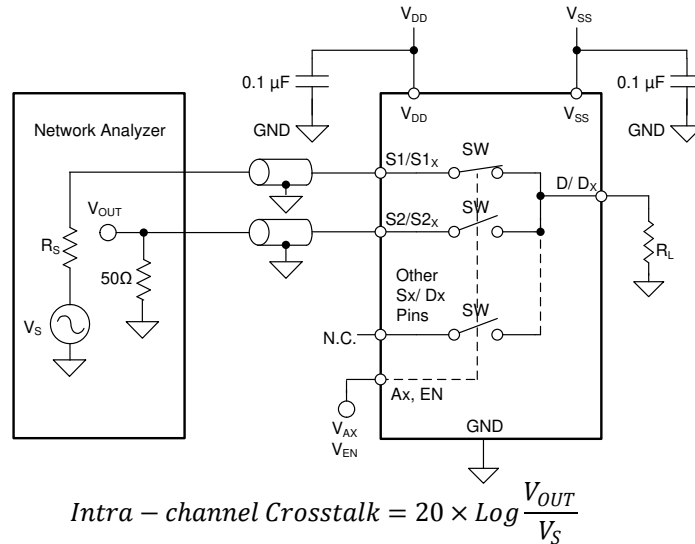
Figure 8-9. Intra-channel Crosstalk Measurement Setup

$$Inter - channel\ Crosstalk = 20 \times Log\frac{V_{OUT}}{V_S}$$
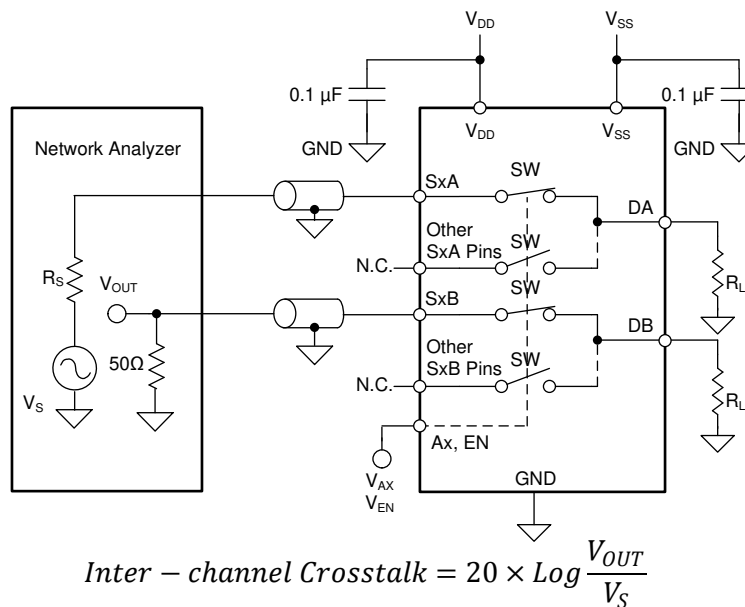
Figure 8-10. Inter-channel Crosstalk Measurement Setup

8.10 Bandwidth

Bandwidth (BW) is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D or Dx) of the TMUX810x. Figure 8-11 shows the setup used to measure bandwidth of the switch.

$$Bandwidth = 20 \times Log\frac{V_{OUT}}{V_S}$$
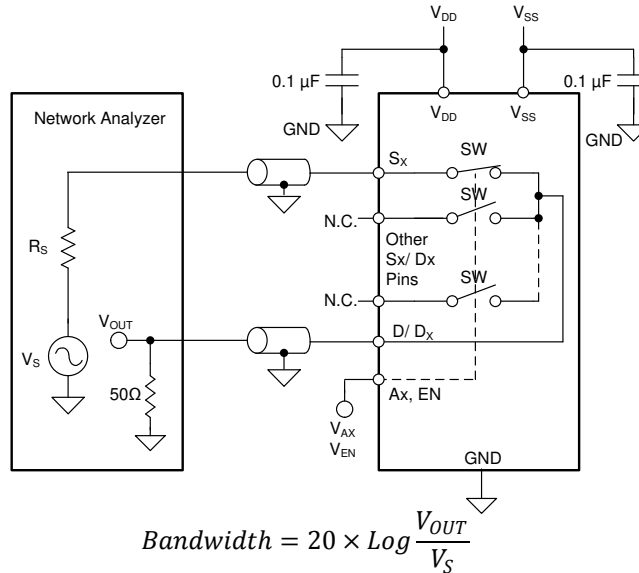
Figure 8-11. Bandwidth Measurement Setup

8.11 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the multiplexer output. The on-resistance of the TMUX8108 and TMUX8109 varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. Figure 8-12 shows the setup used to measure THD+N of the devices.
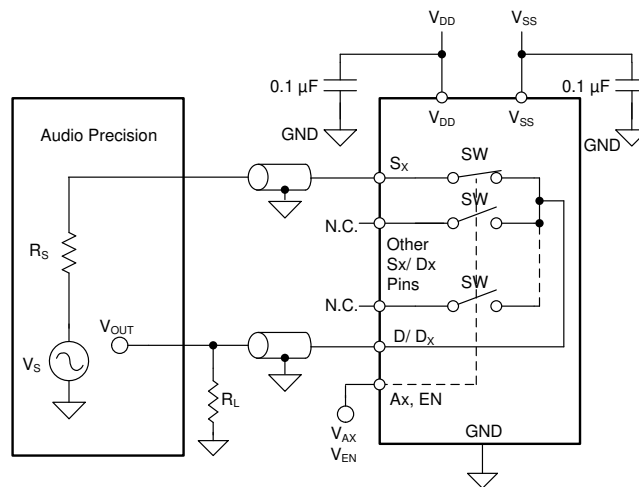
Figure 8-12. THD+N Measurement Setup

9 Detailed Description

9.1 Overview

The TMUX8108 and TMUX8109 are modern complementary metal-oxide semiconductor (CMOS) analog multiplexers in 8:1 (single ended) and 4:1 (differential) configurations. The devices work well with dual supplies, a single supply, or asymmetric supplies up to 100 V.

9.2 Functional Block Diagram
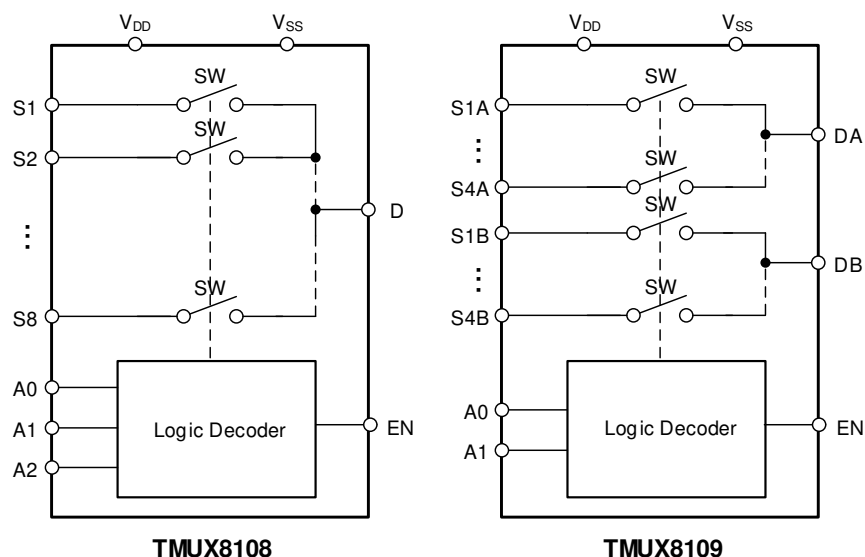
TMUX8108   **TMUX8109**

9.3 Feature Description

9.3.1 Bidirectional Operation

The TMUX8108 and TMUX8109 conduct equally well from source (Sx) to drain (D or Dx) or from drain (D or Dx) to source (Sx). Each signal path has very similar characteristics in both directions.

9.3.2 Flat On – Resistance

The TMUX8108 and TMUX8109 are designed with a special switch architecture to produce ultra-flat on-resistance (R_{ON}) across most of the switch input operating region. The flat R_{ON} response allows the device to be used in precision sensor applications since the R_{ON} is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so no unwanted noise is produced from the device to affect sampling accuracy.

The flatest on-resistance region extends from V_{SS} to roughly 5 V below V_{DD}. Once the signal is within 5 V of V_{DD} the on-resistance will exponentially increase and may impact desired signal transmission.

9.3.3 Protection Features

The TMUX8108 and TMUX8109 offer a number of protection features to enable robust system implementations.

9.3.3.1 Fail-Safe Logic

Fail-safe logic circuitry allows voltages on the logic control pins to be applied before the supply pins, protecting the device from potential damage. Additionaly the fail safe logic feature allows the logic inputs of the mux to be interfaced with high voltages, allowing for simplified interfacing if only high voltage control signals are present. The logic inputs are protected against positive faults of up to +48 V in powered-off condition, but do not offer protection against negative overvoltage condition.

Fail-safe logic also allows the devices to interface with a voltage greater than V_{DD} on the control pins during normal operation to add maximum flexibility in system design. For example, with a V_{DD} = 15 V, the logic control pins could be connected to +24 V for a logic high signal which allows different types of signals, such as analog feedback voltages, to be used when controlling the logic inputs. Regardless of the supply voltage, the logic inputs can be interfaced as high as 48 V.

9.3.3.2 ESD Protection

All pins on the TMUX8108 and TMUX8109 support HBM ESD protection level up to ±2 kV, which helps protect the devices from ESD events during the manufacturing process.

9.3.3.3 Latch-Up Immunity

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

In the TMUX8108 and TMUX8109 devices, an insulating oxide layer is placed on top of the silicon substrate to prevent any parasitic junctions from forming. As a result, the devices are latch-up immune under all circumstances by device construction.

The TMUX8108 and TMUX8109 devices are constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX8108 and TMUX8109 to be used in harsh environments. For more information on latch-up immunity refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability*.

9.3.4 1.8 V Logic Compatible Inputs

The TMUX8108 and TMUX8109 devices have 1.8 V logic compatible control for all logic control inputs. 1.8 V logic level inputs allows the TMUX8108 and TMUX8109 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and bill of materials cost. For more information on 1.8 V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

9.3.5 Integrated Pull-Down Resistor on Logic Pins

The TMUX8108 and TMUX8109 have internal weak pull-down resistors to GND to ensure the logic pins are not left floating. The value of this pull-down resistor is approximately 4 MΩ, but is clamped to about 1 µA at higher voltages. This feature integrates up to four external components and reduces system size and cost.

9.4 Device Functional Modes

9.4.1 Normal Mode

In Normal Mode operation, signals of up to V_{DD} and V_{SS} can be passed through the switch from source (Sx) to drain (D or Dx) or from drain (D or Dx) to source (Sx). Table 9-1 and Table 9-2 shows the address (Ax) pins and the enable (EN) pin determines which switch path to turn on. The following conditions must be satisfied for the switch to stay in the ON condition:

*   The difference between the primary supplies ($V_{DD} - V_{SS}$) must be greater than or equal to 10 V. With a minimum V_{DD} of 10 V.
*   The input signals on the source (Sx) or the drain (Dx) must be be between V_{DD} and V_{SS}.
*   The logic control address pins (Ax) must have selected the switch path.

9.4.2 Truth Tables

Table 9-1 shows the truth tables for the TMUX8108.

Table 9-1. TMUX8108 Truth Table

EN	A2	A1	A0	Normal Condition
0	X[1]	X[1]	X[1]	None
1	0	0	0	S1
1	0	0	1	S2
1	0	1	0	S3
1	0	1	1	S4
1	1	0	0	S5
1	1	0	1	S6
1	1	1	0	S7
1	1	1	1	S8

(1)   "X" means "do not care."

Table 9-2 shows the truth tables for the TMUX8109.

Table 9-2. TMUX8109 Truth Table

EN	A1	A0	Normal Condition
0	X[1]	X[1]	None
1	0	0	S1x
1	0	1	S2x
1	1	0	S3x
1	1	1	S4x

(1)   "X" means "do not care."

If unused, address (Ax) pins must be tied to GND or Logic High in to ensure the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or Dx) should be connected to GND for best performance.

10 Application and Implementation

10.1 Application Information

The TMUX8108 and TMUX8109 are high voltage multiplexers capable of supporting analog and digital signals. The high voltage capability of these multiplexers allow them to be used in systems with high voltage signal swings or in systems with high common mode voltages.

Additionally, the TMUX810x devices provide consistent analog parametric performance across the entire supply voltage range allowing the devices to be powered by the most convient supply rails in the system while still providing excellent performance.

10.2 Typical Application

Many analog front end data acquistion systems are designed to support differential input signals with a wide range of output voltages. In systems where the output sensor is separated from the rest of the signal chain by long cables, a high common mode voltage shift can superimpose on the signal lines. One solution to this problem is to use a high voltage multiplexer in combination with a high voltage op amp level translation stage to properly scale the input signals to the correct input requirements of the ADC. The TMUX8109 allows the system to be designed for a differential, four channel, multiplexed data acquisition system.
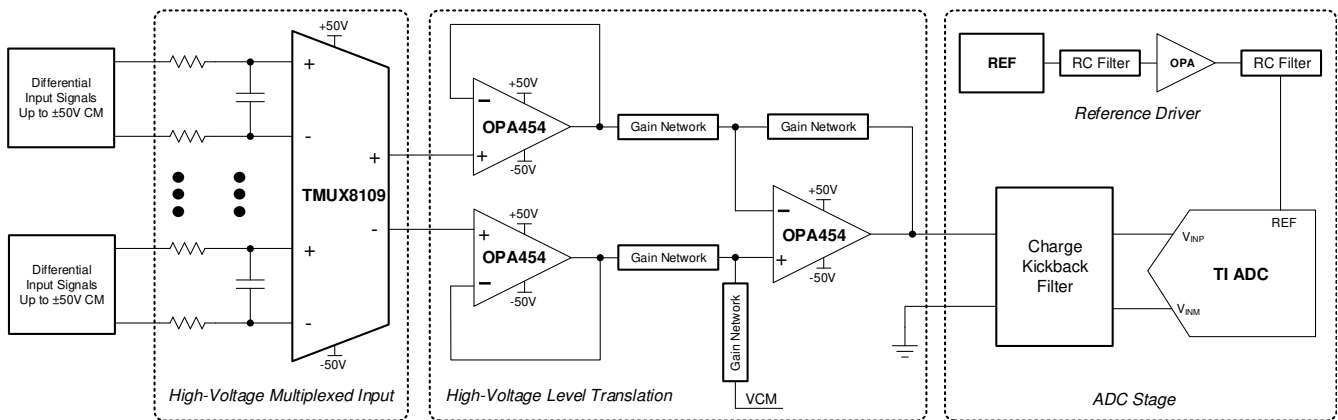

Figure 10-1. Typical Application

10.2.1 Design Requirements

Table 10-1. Design Parameters

PARAMETER	VALUE
Positive supply (V_{DD}) mux and Op Amps	+50 V
Negative supply (V_{SS}) mux and Op Amps	-50 V
Maximum input / output signals with common mode shift	-50 V to 50 V
Mux control logic thresholds	1.8 V compatible, up to 48 V
Mux temperature range	-40°C to +125°C

10.2.2 Detailed Design Procedure

The multiplexed data aquistion circuit allows the system designer to have flexibility over both size and cost of the end product. Utilizing a multiplexer can reduce board size and cost by reducing the number of op amp circuits required for a multi-channel design. Additionally, the high voltage multiplexer can be paired with many implementations of high voltage level translation circuits such as difference amplifiers, instrumentation amplifiers, or fully differential amplifiers depending on the gain, noise requirements, and cost targets of the system.

In the example application, the TMUX8109 is paired with a difference amplifier and buffer stage op amps on both the positive and negative differential signals. Many data aquistion systems will place a buffer op amp following the mux for two reasons. The first reason is to eliminate the impact of the multiplexer on-resistance change across the signal range, preventing gain errors in the system. Secondly, depending on the output impedance of the sensors being interfaced, a high input impedance stage may be required to achieve system specification targets. The TMUX810x multiplexers have exceptionally flat on-resistance and low leakge currents across the signal voltage range and can potentially eliminate the need for buffer stage op amps depending on system requirements. Additionally, excellent crosstalk and off-isolation performance, paired with low capacitance ratings makes the TMUX810x multiplexers very flexible for system design of data aquistion systems.

A difference amplifier stage follows the multiplexer to eliminate the common mode voltage shift and can be used to scale the input signals to match the dynamic range of the selected ADC. In this example, both the op amp and multiplexer are rated for performance up to ±50 V. To find the maximum common mode voltage shift allowed, the system designer should take the maximum supply voltage and subtract the maximum voltage of the differential signal; the resulting voltage is the maximum common mode shift that can be accomodated without exceding the input voltage requirements of the multiplexer. The difference amplifier circuit relies on the matched resistor for good CMRR performance and typically has lower voltage gains and lower input impedances. If higher gains are required, or for better CMRR performance, an instrumentation amplifier can be swapped into the circuit. Both op amp solutions can be utilized to remove the common mode voltage offset and extract the true differential signal. The high voltage multiplexer at the front end of the design requires the system to have high voltage power supply rails to pass signals within V_{SS} and V_{DD}, this should be considered in the overal architecture of the system design. This multiplexed application becomes increasingly valuable with larger number of input channels by greatly reducing the total component count.

Product Folder Links: TMUX8108 TMUX8109

10.2.3 Application Curves

The example application utilizes the excellent leakage and crosstalk performance of the TMUX810x devices to reduce any impact introduced from a multiplexed system architecture. Figure 10-2 shows the leakage current for both ON and OFF cases with a varrying temperature. Figure 10-3 shows the excellent crosstalk performance of the TMUX810x devices. These features make the TMUX8108 and TMUX8109 an ideal solution for multiplexed data acquisition applications that require excellent linearity and low distortion.
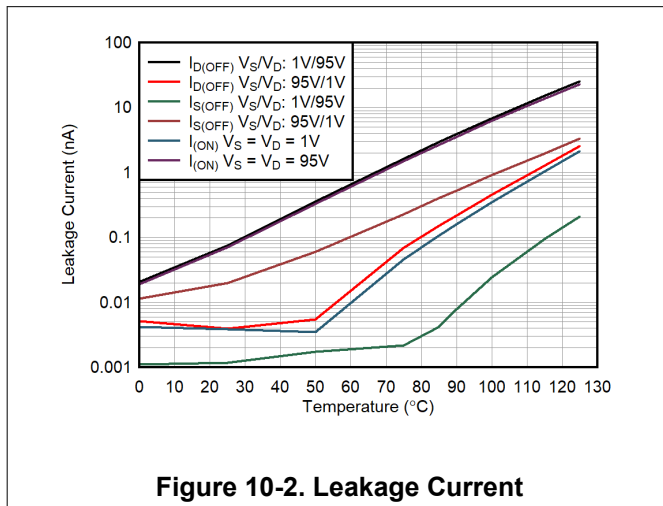
Figure 10-2. Leakage Current
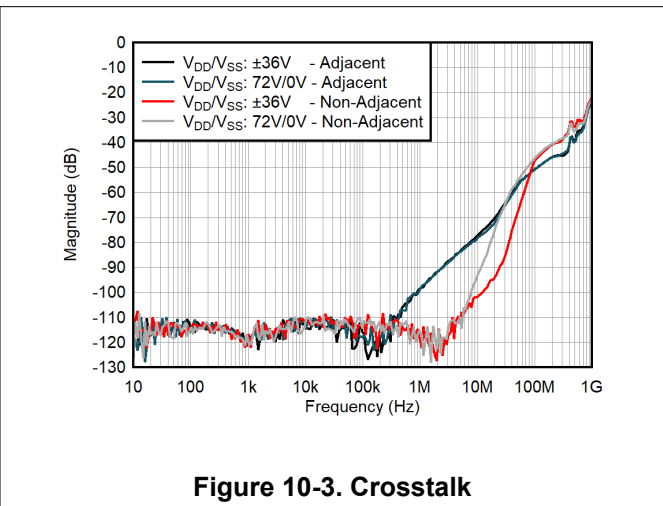
Figure 10-3. Crosstalk

11 Power Supply Recommendations

The TMUX8108 and TMUX8109 operate across a wide supply range of ±10 V to ±50 V (10 V to 100 V in single-supply mode). They also perform well with asymmetric supplies such as V_{DD} = 50 V and V_{SS}= –10 V. For improved supply noise immunity, use a supply decoupling capacitor ranging from 1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. An additional 0.1 µF capacitor placed closest to the supply pins will provide the best supply decoupling solution. Always ensure the ground (GND) connection is established before supplies are ramped.

12 Layout
12.1 Layout Guidelines

The following images illustrate an example of a PCB layout with the TMUX8108 and TMUX8109. Some key considerations are:

- For reliable operation, connect at least one decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and V_{SS} to GND. We recommend a 0.1 µF and 1 µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
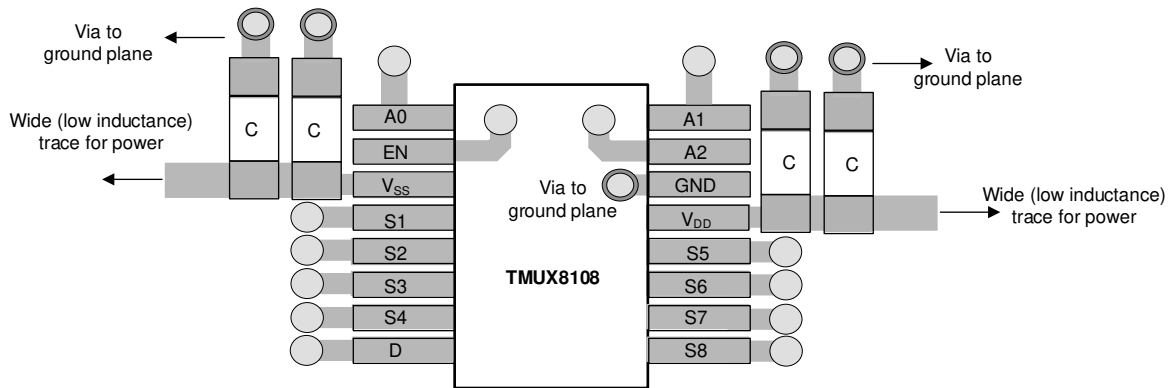
12.2 Layout Example

Figure 12-1. TMUX8108 TSSOP Layout Example

Figure 12-2. TMUX8108 QFN Layout Example
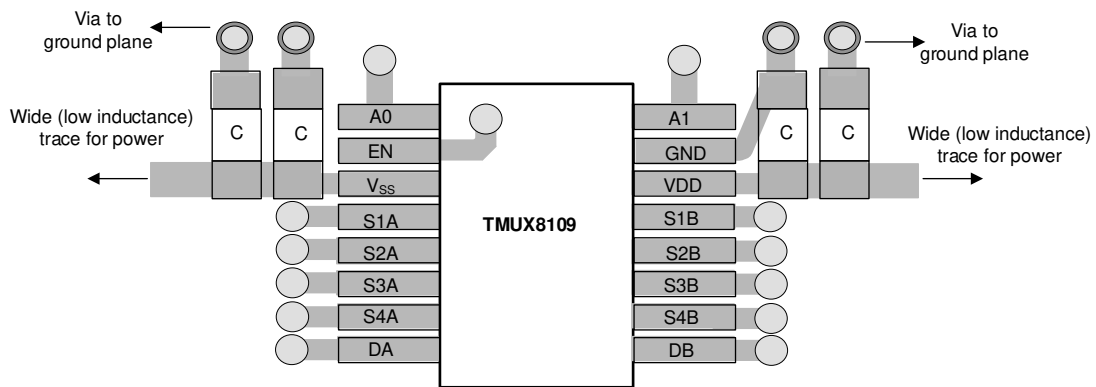
Figure 12-3. TMUX8109 TSSOP Layout Example

Figure 12-4. TMUX8109 QFN Layout Example

Product Folder Links: *TMUX8108 TMUX8109*

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note
- Texas Instruments, *Multiplexers and Signal Switches Glossary* application report
- Texas Instruments, *Using Latch-Up Immune Multiplexers to Help Improve System Reliability* application report
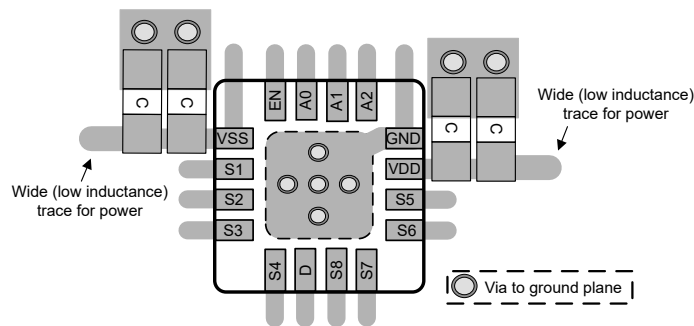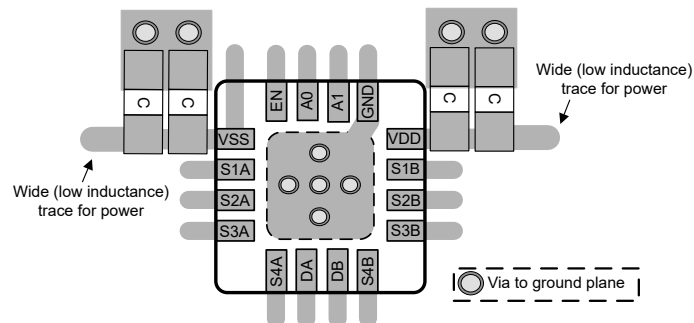
13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 Trademarks

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTMUX8108PWR	ACTIVE	TSSOP	PW	16	2000	TBD	Call TI	Call TI	-40 to 125		Samples
PTMUX8109PWR	ACTIVE	TSSOP	PW	16	2000	TBD	Call TI	Call TI	-40 to 125		Samples
TMUX8108PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM8108	Samples
TMUX8109PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM8109	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX8108PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX8109PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX8108PWR	TSSOP	PW	16	2000	853.0	449.0	35.0
TMUX8109PWR	TSSOP	PW	16	2000	853.0	449.0	35.0

4220204/A   02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

16X (1.5)

SYMM

1

16X (0.45)

(R0.05) TYP

16

SYMM

14X (0.65)

8

9

(5.8)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A   02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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