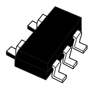
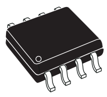
TSZ181H1, TSZ182H1

Datasheet

Very high accuracy (70 µV), high bandwidth (3 MHz), high temperature (175 °C), zero-drift operational amplifiers


SOT23-5


SO8

Maturity status link
TSZ181H1, TSZ182H1

Related products	
TSZ181H, TSZ182H	For - 40 / 150 °C range
TSZ181, TSZ182	For - 40 / 125 °C range

Features

- AEC-Q100 qualified
- Very high accuracy and stability:
  - 70 µV max. offset voltage at 25 °C
  - 100 µV offset voltage over full temperature range
- Rail-to-rail input and output
- Low supply voltage: 2.2 - 5.5 V
- Low power consumption: 1 mA max. at 5 V
- Gain bandwidth product: 3 MHz
- Automotive qualification
- Extended temperature range: -40 to 175 °C
- Micropackage: SOT23-5, SO8
- Benefits:
  - Higher accuracy without calibration
  - Accuracy virtually unaffected by temperature change

Applications

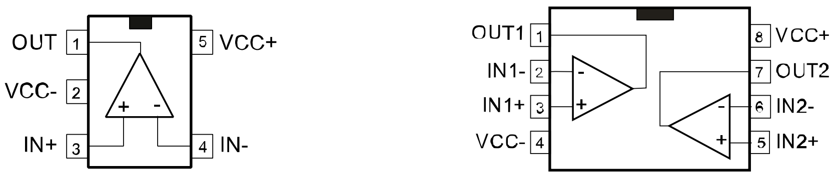
- High accuracy signal conditioning
- Current measurement
- Sensor signal conditioning
- Automotive

Description

The TSZ181H1 single and TSZ182H1 dual operational amplifiers feature very low offset voltages with virtually zero drift versus temperature changes. The TSZ181H1 and TSZ182H1 offer rail-to-rail input and output, excellent speed/power consumption ratio, and 3 MHz gain bandwidth product, while consuming just 1 mA at 5 V. The device operates over an extended range of -40 to +175°C and features an ultra-low input bias current. These features make the TSZ181H1 and TSZ182H1 ideal for high-accuracy high-bandwidth sensor interfaces for automotive environment.

1 Pin connections

Figure 1. Pin connections (top view)



SOT23-5 (TSZ181H1) SO8 (TSZ182H1)

2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage (1)	6	V
V_{id}	Differential input voltage (2)	± V_{cc}	V
V_{in}	Input voltage (3)	(V_{cc-}) - 0.2 to (V_{cc+}) + 0.2	V
I_{in}	Input current (4)	10	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_j	Junction temperature	180	°C
$R_{th\text{-}ja}$	Thermal resistance junction to ambient (5) (6) SO8 SOT23-5	 125 250	°C/W
ESD	Human Body Model (HBM) (7)	4	kV
	Charged Device Model (CDM) (8)	1.5	

1. *All voltage values, except differential voltage, are with respect to network ground terminal.*
2. *The differential voltage is the non-inverting input terminal with respect to the inverting input terminal.*
3. *V_{CC} - V_{in} must not exceed 6 V, V_{in} must not exceed 6 V.*
4. *Input current must be limited by a resistor in series with the inputs.*
5. *R_{th} are typical values.*
6. *Short-circuits can cause excessive heating and destructive dissipation.*
7. *Human body model: 100 pF discharged through a 1.5 kΩ resistor between two pins of the device, done for all couples of pin combinations with other pins floating.*
8. *Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.*

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{cc}	Supply voltage	2.2 to 5.5	V
V_{icm}	Common mode voltage on input pins	(V_{cc-}) - 0.1 to (V_{cc+}) + 0.1	V
T	Operating free-air temperature range	-40 to 175	°C

3 Electrical characteristics

Table 3. Electrical characteristics at Vcc+ = 2.2 V, Vcc- = 0 V, Vicm = Vcc/2, T = 25 °C, R_L = 10 kΩ connected to Vcc/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC performance						
V_{IO}	Input offset voltage	T = 25 °C		3.5	70	µV
		Tmin < T < Tmax			100	
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift (1)	Tmin < T < Tmax			0.26	µV/°C
I_{IB}	Input bias current (V_{OUT} = V_{CC}/2) (2)	T = 25 °C		30	200	pA
		Tmin < T < Tmax		225		
I_{IO}	Input offset current (V_{OUT} = V_{CC}/2) (2)	T = 25 °C		60	400	
		Tmin < T < Tmax		150		
CMR1	Common-mode rejection ratio (3), V_{ic} = 0 V to V_{CC}, V_{OUT} = V_{cc}/2, R_L > 1 MΩ	T = 25 °C	88	115		dB
		Tmin < T < Tmax	86			
A_{vd}	Large signal voltage gain, V_{OUT} = 0.5 V to (V_{CC} - 0.5 V)	T = 25 °C	102	130		
		Tmin < T < Tmax	92			
V_{OH}	High-level output voltage, V_{OH} = V_{CC} - V_{OUT}	T = 25 °C		15	40	mV
		Tmin < T < Tmax			70	
V_{OL}	Low-level output voltage	T = 25 °C		10	30	
		Tmin < T < Tmax			70	
I_{OUT}	I_{sink} (V_{OUT} = V_{CC})	T = 25 °C	4	6		mA
		Tmin < T < Tmax	1.87			
	I_{source} (V_{OUT} = 0 V)	T = 25 °C	3.5	4		
		Tmin < T < Tmax	1.4			
I_{CC}	Supply current per channel, V_{OUT} = V_{CC} /2, R_L > 1 MΩ	T = 25 °C		0.7	1	
		Tmin < T < Tmax			1.2	
AC performance						
GBP	Gain bandwidth product, R_L = 10 kΩ, C_L = 100 pF	T = 25 °C	1.6	2.3		MHz
		Tmin < T < Tmax	1			
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		59		degrees
G_m	Gain margin			16		dB
SR	Slew rate (4)	T = 25 °C	3	4.6		V/µs
		Tmin < T < Tmax	2.5			
t_s	Settling time	To 0.1%, V_{in} = 0.8 Vpp		500		ns
e_n	Equivalent input noise voltage density	f = 1 kHz		50		nV/√Hz
		f = 10 kHz		50		
e_{n-pp}	Voltage noise	f = 0.1 to 10 Hz		0.6		µVpp
C_S	Channel separation	f = 1 kHz		120		dB
t_{init}	Initialization time, G = 100 (5)	T = 25 °C		60		µs
		Tmin < T < Tmax		120		

1. *Input offset measurements are performed on x100 gain configuration. The amplifiers and the gain setting resistors are at the same temperature.*
2. *Guaranteed by design.*
3. *CMR is defined as 20xLOG($\Delta V_{icm}/\Delta V_{io}$).*
4. *Slew rate value is calculated as the average between positive and negative slew rates.*
5. *Initialization time is defined as the delay between the moment when supply voltage exceeds 2.2 V and output voltage stabilization.*

Table 4. Electrical characteristics at Vcc+ = 3.3 V, Vcc- = 0 V, Vicm = Vcc/2, T = 25 °C, R_L = 10 kΩ connected to Vcc/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC performance						
V_{IO}	Input offset voltage	T = 25 °C		2	70	µV
		Tmin < T < Tmax			100	
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift [(1)]	Tmin < T < Tmax			0.26	µV/°C
I_{IB}	Input bias current (V_{OUT} = V_{CC}/2) [(2)]	T = 25 °C		30	200	pA
		Tmin < T < Tmax		225		
I_{IO}	Input offset current (V_{OUT} = V_{CC}/2) [(2)]	T = 25 °C		60	400	
		Tmin < T < Tmax		150		
CMR1	Common-mode rejection ratio [(3)], V_{ic} = 0 V to V_{CC}, V_{OUT} = V_{cc}/2, R_L > 1 MΩ	T = 25 °C	96	120		dB
		Tmin < T < Tmax	94			
CMR2	Common-mode rejection ratio [(3)], V_{OUT} = V_{cc}/2, R_L > 1 MΩ	T = 25 °C, V_{ic} = 0 to V_{CC} - 1.8 V	109	132		
		Tmin < T < Tmax, V_{ic} = 0 to V_{CC} - 2 V	103			
A_{vd}	Large signal voltage gain, V_{OUT} = 0.5 V to (V_{CC} - 0.5 V)	T = 25 °C	110	138		
		Tmin < T < Tmax	95			
V_{OH}	High-level output voltage, V_{OH} = V_{CC} - V_{OUT}	T = 25 °C		16	40	mV
		Tmin < T < Tmax			70	
V_{OL}	Low-level output voltage	T = 25 °C		11	30	
		Tmin < T < Tmax			70	
I_{OUT}	I_{sink} (V_{OUT} = V_{CC})	T = 25 °C	10	15		mA
		Tmin < T < Tmax	6.1			
	I_{source} (V_{OUT} = 0 V)	T = 25 °C	6	11		
		Tmin < T < Tmax	2.8			
I_{CC}	Supply current per channel, V_{OUT} = V_{CC} /2, R_L > 1 MΩ	T = 25 °C		0.7	1	
		Tmin < T < Tmax			1.2	
AC performance						
GBP	Gain bandwidth product, R_L = 10 kΩ, C_L = 100 pF	T = 25 °C	2	2.8		MHz
		Tmin < T < Tmax	1.2			
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		56		degrees
G_m	Gain margin			15		dB
SR	Slew rate [(4)]	T = 25 °C	2.6	4.5		V/µs
		Tmin < T < Tmax	2.1			
t_s	Settling time	To 0.1%, V_{in} = 1.2 Vpp		550		ns
e_n	Equivalent input noise voltage density	f = 1 kHz		40		nV/√Hz
		f = 10 kHz		40		
e_{n-pp}	Voltage noise	f = 0.1 to 10 Hz		0.5		µVpp
C_S	Channel separation	f = 1 kHz		120		dB
t_{init}	Initialization time, G = 100 [(5)]	T = 25 °C		60		µs
		Tmin < T < Tmax		120		

1. *Input offset measurements are performed on x100 gain configuration. The amplifiers and the gain setting resistors are at the same temperature.*
2. *Guaranteed by design.*
3. *CMR is defined as 20xLOG($\Delta V_{icm}/\Delta V_{io}$)*
4. *Slew rate value is calculated as the average between positive and negative slew rates.*
5. *Initialization time is defined as the delay between the moment when supply voltage exceeds 2.2 V and output voltage stabilization.*

Table 5. Electrical characteristics at Vcc+ = 5 V, Vcc- = 0 V, Vicm = Vcc/2, T = 25 °C, R_L = 10 kΩ connected to Vcc/2 (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DC performance						
V_{IO}	Input offset voltage	T = 25 °C		1	70	µV
		Tmin < T < Tmax			100	
$\|\Delta V_{IO}/\Delta T\|$	Input offset voltage drift (5)	Tmin < T < Tmax			0.26	µV/°C
I_{IB}	Input bias current ($V_{OUT} = V_{CC}/2$) (2)	T = 25 °C		30	200	pA
		Tmin < T < Tmax		225		
I_{IO}	Input offset current ($V_{OUT} = V_{CC}/2$) (2)	T = 25 °C		60	400	
		Tmin < T < Tmax		150		
CMR1	Common-mode rejection ratio (3), V_{ic} = 0 V to V_{CC}, $V_{OUT} = V_{cc}/2$, R_L > 1 MΩ	T = 25 °C	103	126		dB
		Tmin < T < Tmax	101			
CMR2	Common-mode rejection ratio (3), $V_{OUT} = V_{cc}/2$, R_L > 1 MΩ	T = 25 °C, V_{ic} = 0 to V_{CC} - 1.8 V	112	136		
		Tmin < T < Tmax, V_{ic} = 0 to V_{CC} - 2 V	106			
SVR1	Supply voltage rejection ratio (4), V_{cc} = 2.2 to 5.5 V, V_{ic} = 0 V, R_L > 1 MΩ	T = 25 °C	101	123		
		Tmin < T < Tmax	99			
A_{vd}	Large signal voltage gain, V_{OUT} = 0.5 V to (V_{CC} - 0.5 V)	T = 25 °C	110	144		
		Tmin < T < Tmax	104			
EMIRR	EMI rejection ratio (5)	V_{RF} = 100 mVp, f = 400 MHz		52		
		V_{RF} = 100 mVp, f = 900 MHz		52		
		V_{RF} = 100 mVp, f = 1800 MHz		72		
		V_{RF} = 100 mVp, f = 2400 MHz		85		
V_{OH}	High-level output voltage, $V_{OH} = V_{CC} - V_{OUT}$	T = 25 °C		18	40	mV
		Tmin < T < Tmax			70	
V_{OL}	Low-level output voltage	T = 25 °C		13	30	
		Tmin < T < Tmax			70	
I_{OUT}	I_{sink} ($V_{OUT} = V_{CC}$)	T = 25 °C	20	29		mA
		Tmin < T < Tmax	12			
	I_{source} (V_{OUT} = 0 V)	T = 25 °C	15	25		
		Tmin < T < Tmax	7			
I_{CC}	Supply current per channel, $V_{OUT} = V_{CC}/2$, R_L > 1 MΩ	T = 25 °C		0.8	1	
		Tmin < T < Tmax			1.2	
AC performance						
GBP	Gain bandwidth product, R_L = 10 kΩ, C_L = 100 pF	T = 25 °C	2	3		MHz
		Tmin < T < Tmax	1.2			

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Φ_m	Phase margin	R_L = 10 kΩ, C_L = 100 pF		56		degrees
G_m	Gain margin			15		dB
SR	Slew rate [6]	T = 25 °C	2.9	4.7		V/μs
		Tmin < T < Tmax	2.4			
t_s	Settling time	To 0.1%, V_{in} = 1.5 Vpp		600		ns
		To 0.01%, V_{in} = 1 Vpp		4		μs
e_n	Equivalent input noise voltage density	f = 1 kHz		37		nV/√Hz
		f = 10 kHz		37		
e_{n-pp}	Voltage noise	f = 0.1 to 10 Hz		0.4		μVpp
C_S	Channel separation	f = 100 Hz		135		dB
t_{init}	Initialization time, G = 100 [7]	T = 25 °C		60		μs
		Tmin < T < Tmax		100		

1. *Input offset measurements are performed on x100 gain configuration. The amplifiers and the gain setting resistors are at the same temperature.*
2. *Guaranteed by design.*
3. *CMR is defined as 20xLOG($\Delta V_{icm}/\Delta V_{io}$).*
4. *SVR is defined as 20xLOG($\Delta V_{cc}/\Delta V_{io}$).*
5. *EMIRR is defined as -20Log($V_{RF\_Peak}/\Delta V_{io}$), Tested on the MiniSO8 package, RF injection on the IN- pin.*
6. *Slew rate value is calculated as the average between positive and negative slew rates.*
7. *Initialization time is defined as the delay between the moment when supply voltage exceeds 2.2 V and output voltage stabilization.*

4 Typical performance characteristics

Figure 2. Supply current vs. supply voltage

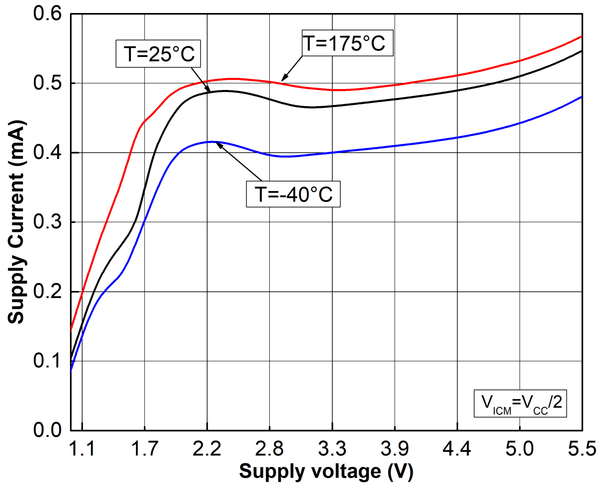


Figure 3. Input offset voltage distribution at V_{CC} = 5 V

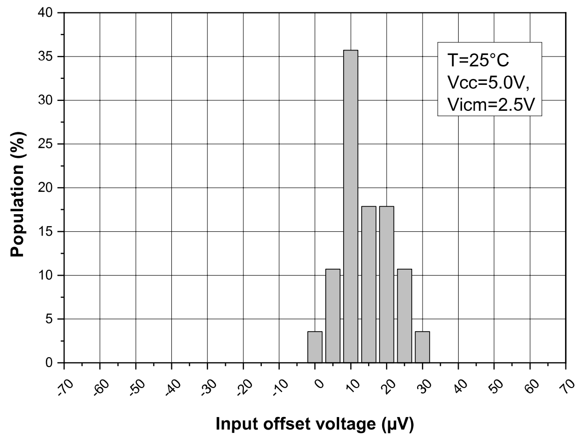


Figure 4. Input offset voltage distribution at V_{CC} = 3.3 V

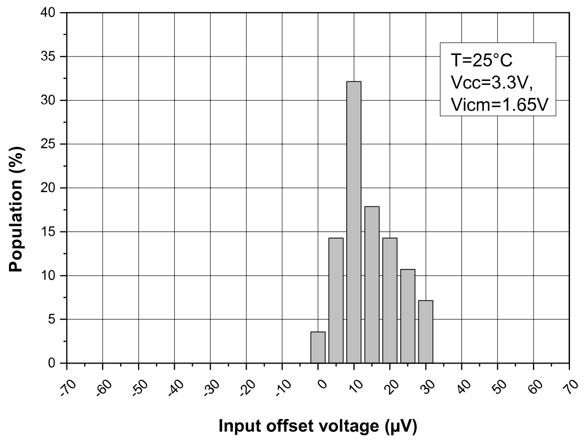


Figure 5. Input offset voltage distribution at V_{CC} = 2.2 V

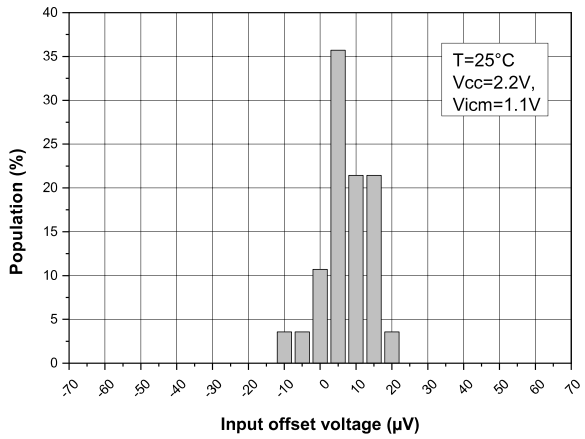


Figure 6. Input offset voltage distribution at V_{CC} = 5 V, T = 175 °C

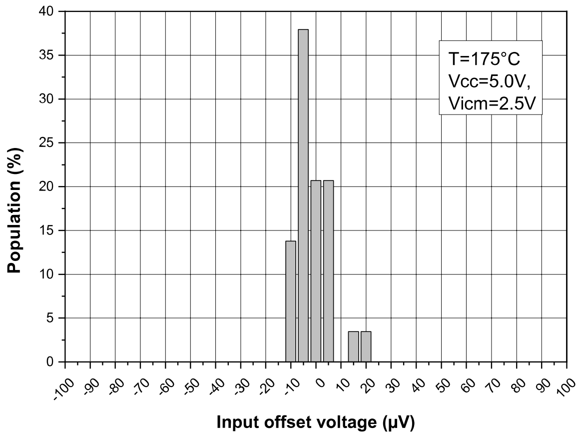


Figure 7. Input offset voltage distribution at V_{CC} = 5 V, T = -40 °C

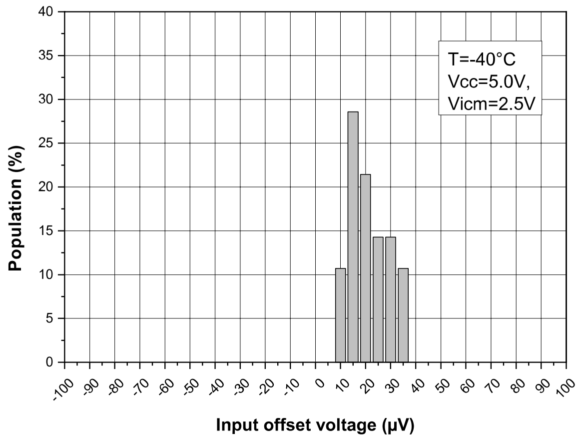


Figure 8. Input offset voltage distribution at V_{CC} = 2.2 V, T = 175 °C

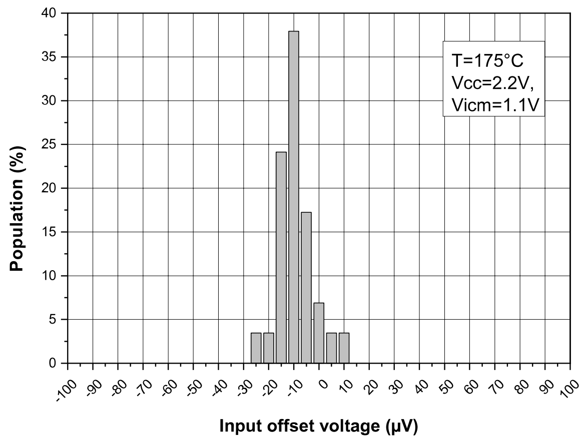


Figure 9. Input offset voltage distribution at V_{CC} = 2.2 V, T = -40 °C

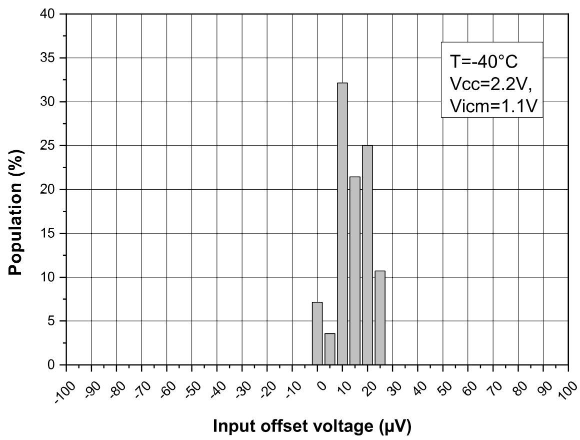


Figure 10. Input offset voltage vs. supply voltage

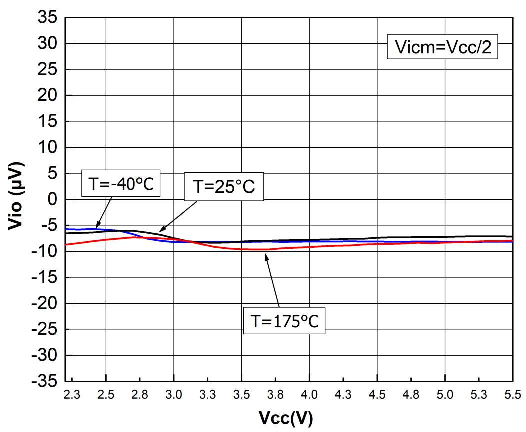


Figure 11. Input offset voltage vs. input common mode at V_{CC} = 5.5 V

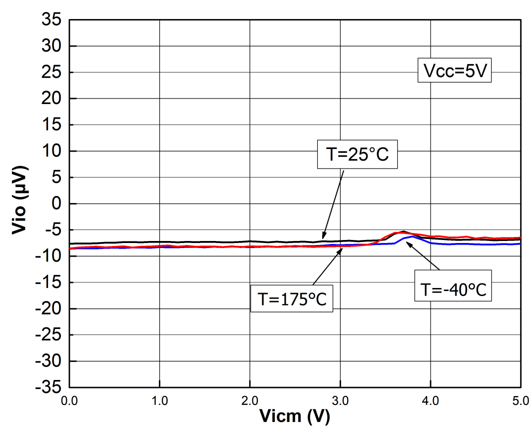


Figure 12. Input offset voltage vs. input common mode at V_{CC} = 3.3 V

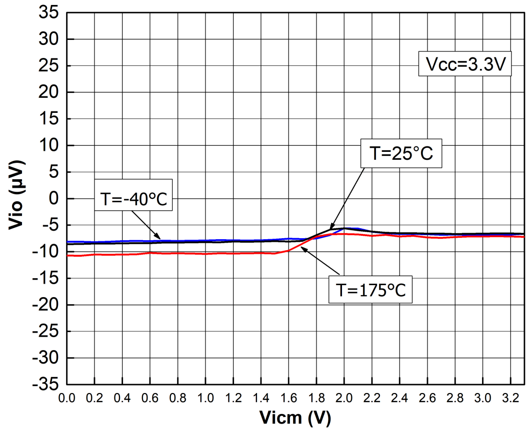


Figure 13. Input offset voltage vs. input common mode at V_{CC} = 2.2 V

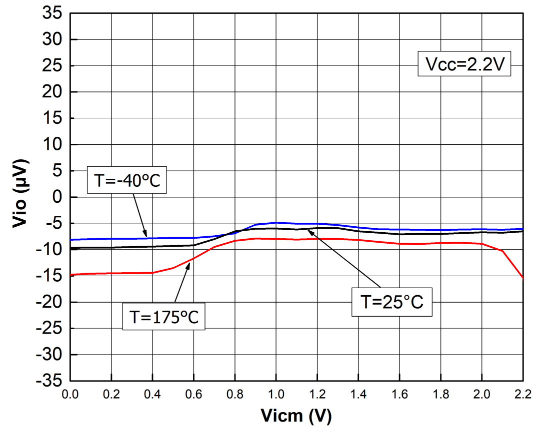


Figure 14. Input offset voltage vs. temperature

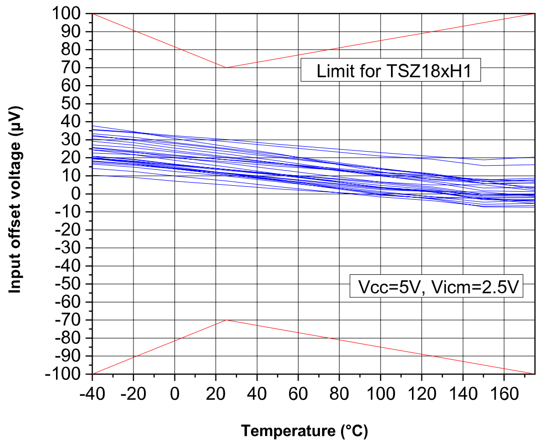


Figure 15. V_{OH} vs. supply voltage

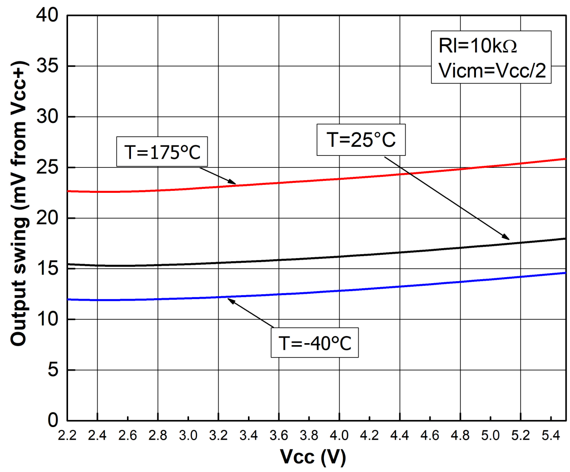


Figure 16. V_{OL} vs. supply voltage

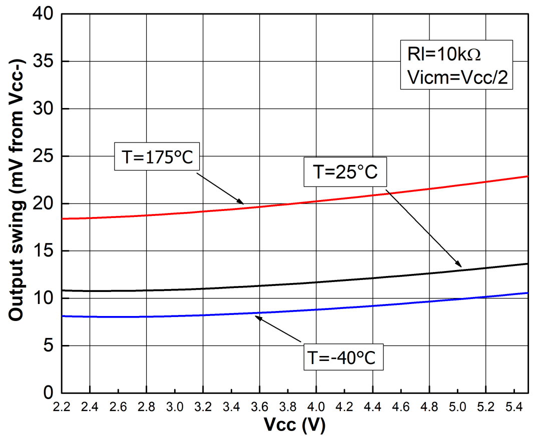


Figure 17. Output current vs. output voltage at V_{CC} = 5 V

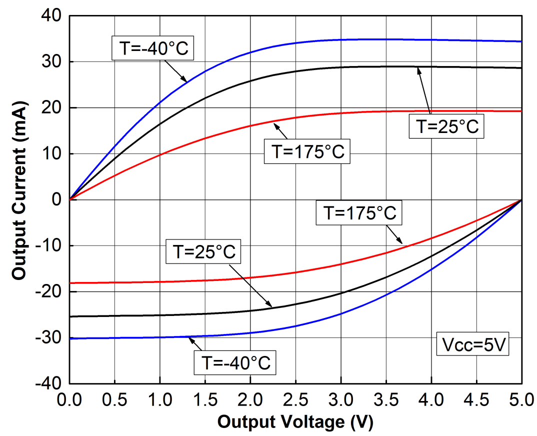


Figure 18. Output current vs. output voltage at V_{CC} = 2.2 V

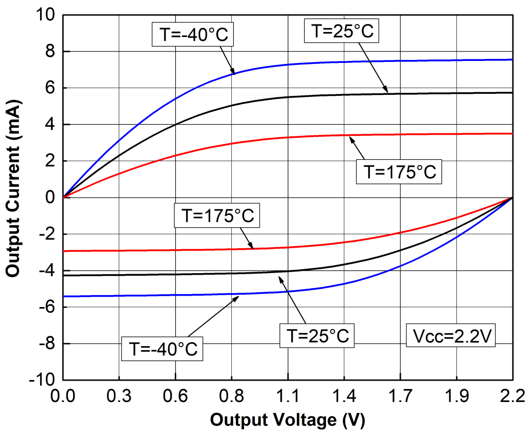


Figure 19. Input bias current vs. common-mode at V_{CC} = 5 V

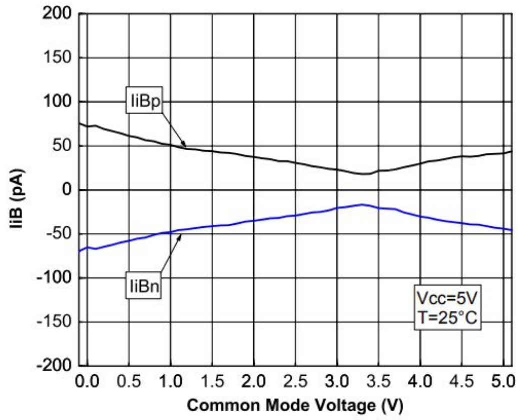


Figure 20. Input bias current vs. temp. at V_{CC} = 5 V

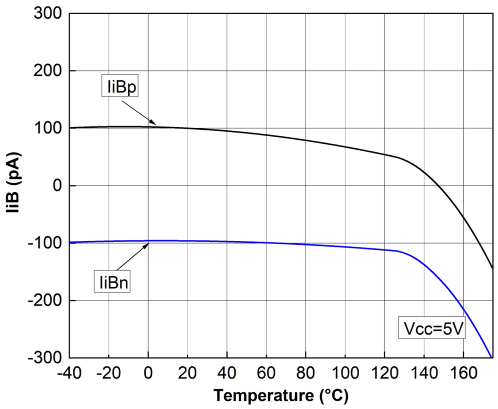


Figure 21. Output rail linearity

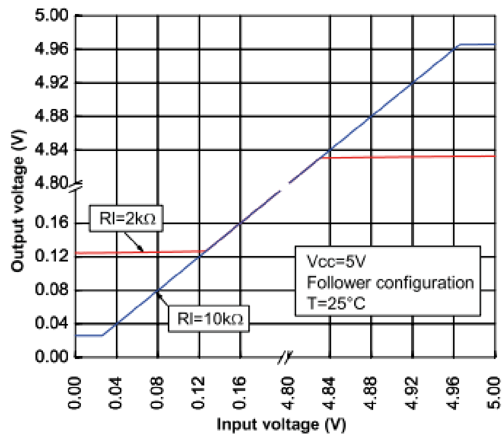


Figure 22. Bode diagram at V_{CC} = 5 V

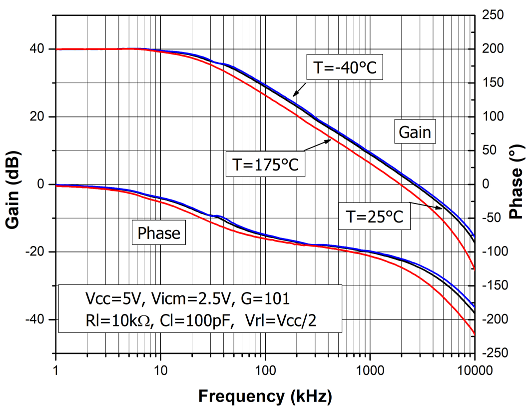


Figure 23. Bode diagram at V_{CC} = 2.2 V

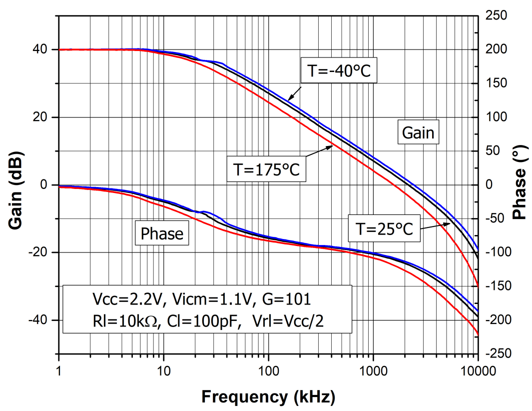


Figure 24. Bode diagram at V_{CC} = 3.3 V

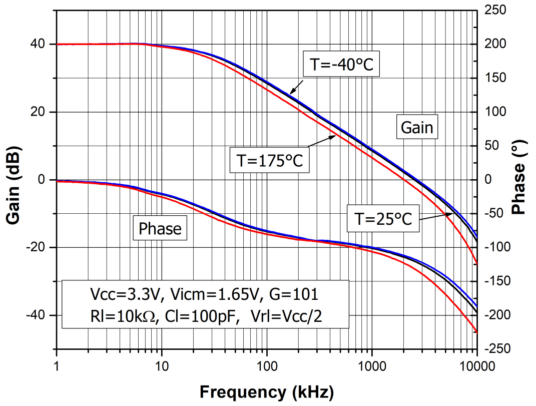


Figure 25. Open loop gain vs. frequency

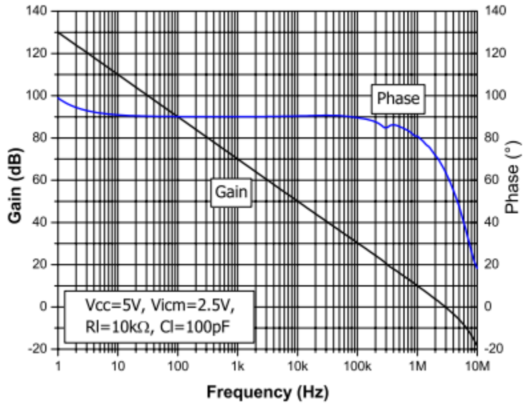


Figure 26. Positive slew rate vs. supply voltage

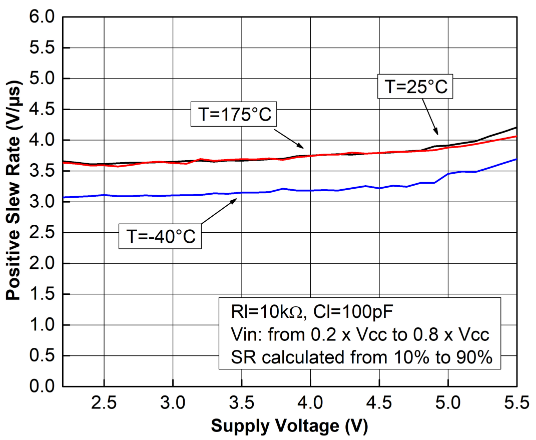


Figure 27. Negative slew rate vs. supply voltage

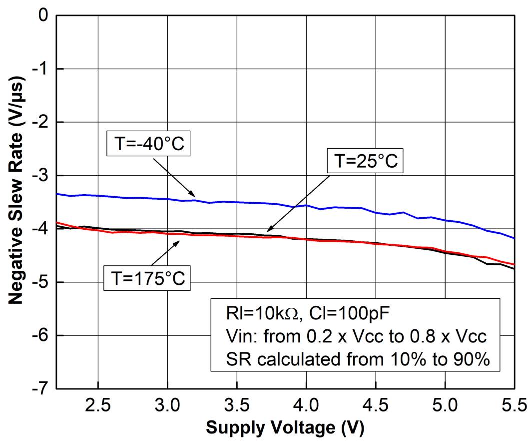


Figure 28. Noise 0.1 – 10 Hz vs. time

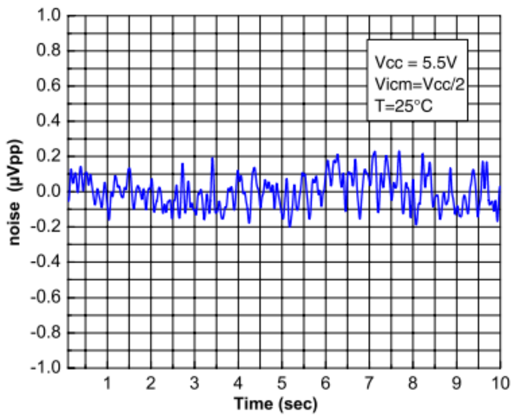
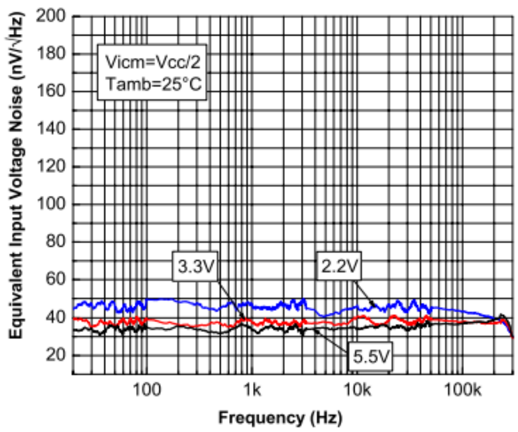


Figure 29. Noise vs. frequency



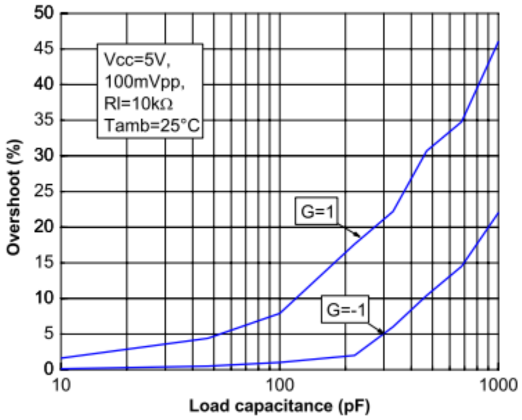


Figure 30. Output overshoot vs. load capacitance

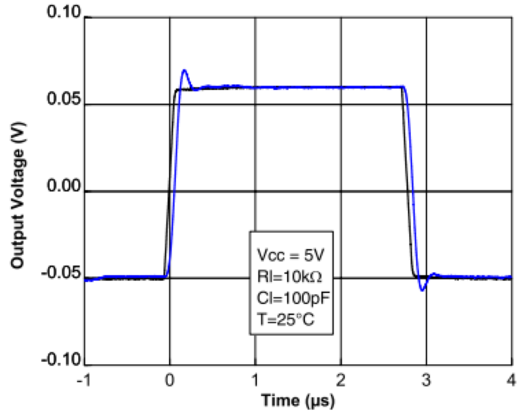


Figure 31. Small signal V_{CC} = 5 V

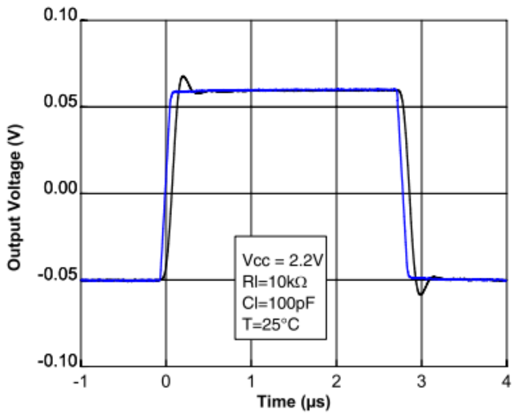


Figure 32. Small signal V_{CC} = 2.2 V

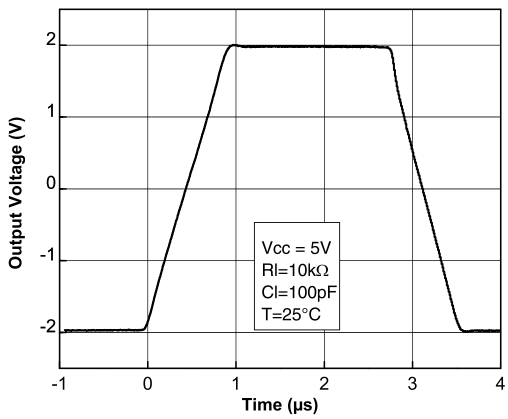


Figure 33. Large signal V_{CC} = 5 V

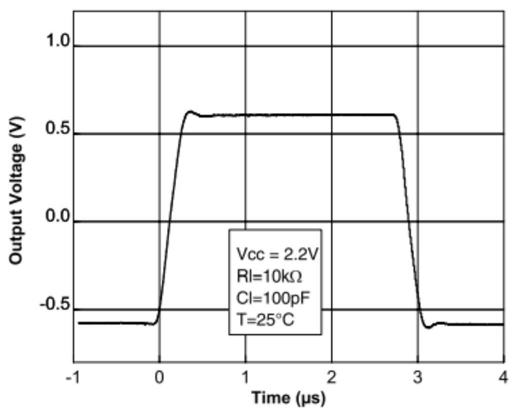


Figure 34. Large signal V_{CC} = 2.2 V

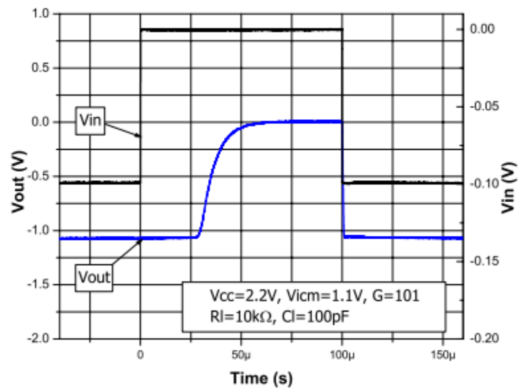


Figure 35. Negative overv. recovery V_{CC} = 2.2 V

Figure 36. Positive overvoltage recovery V_{CC} = 5 V

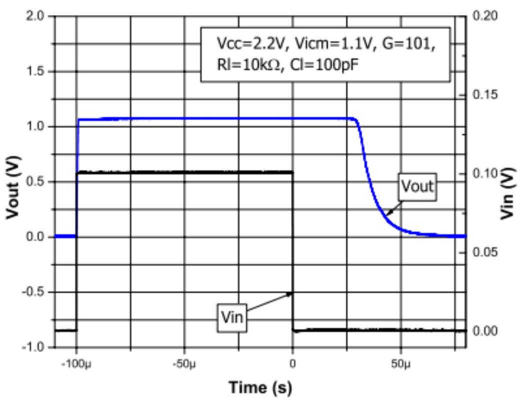


Figure 37. Output impedance vs. frequency

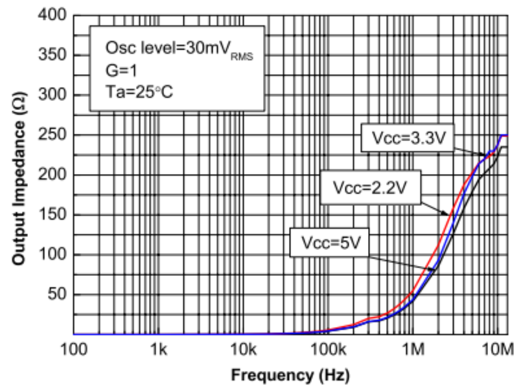


Figure 38. Settling time positive step (-2 V to 0 V)

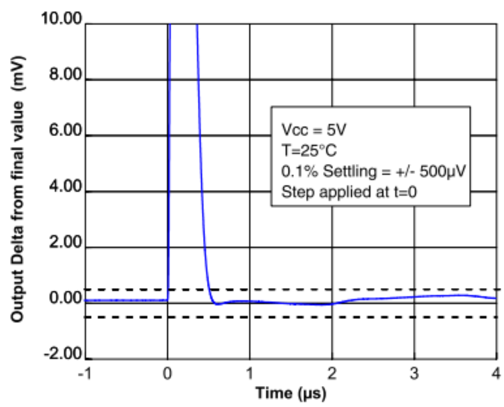


Figure 39. Settling time negative step (2 V to 0 V)

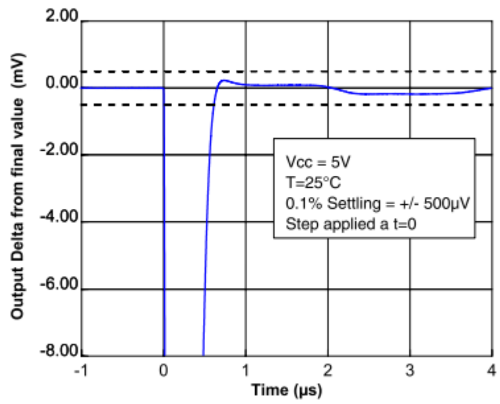


Figure 40. Settling time positive step (-0.8 V to 0 V)

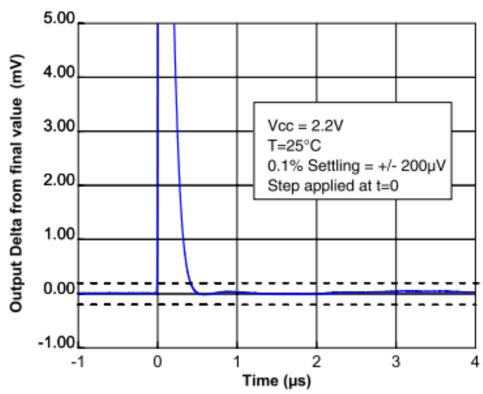


Figure 41. Settling time negative step (0.8 V to 0 V)

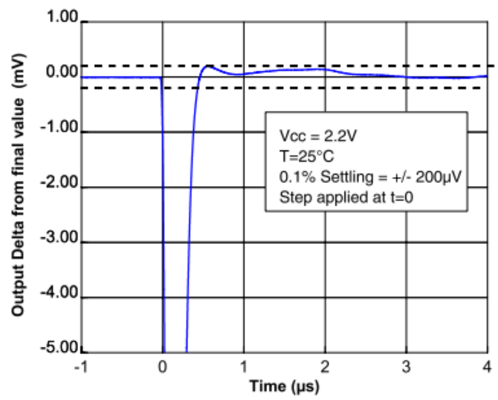


Figure 42. **Maximum output voltage vs. frequency**

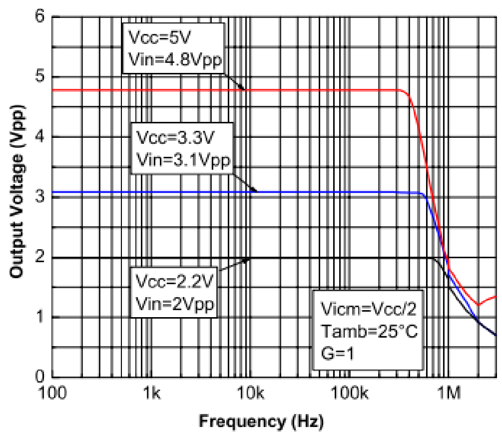


Figure 43. **Crosstalk vs. frequency**

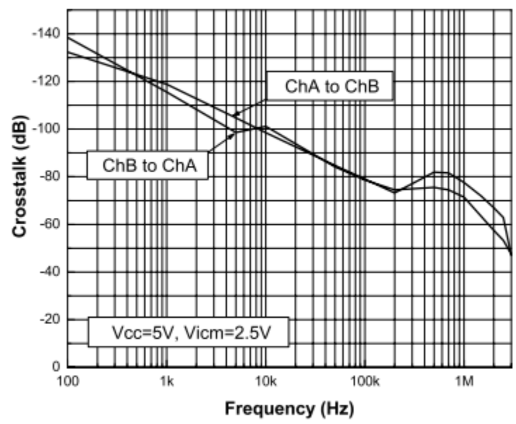
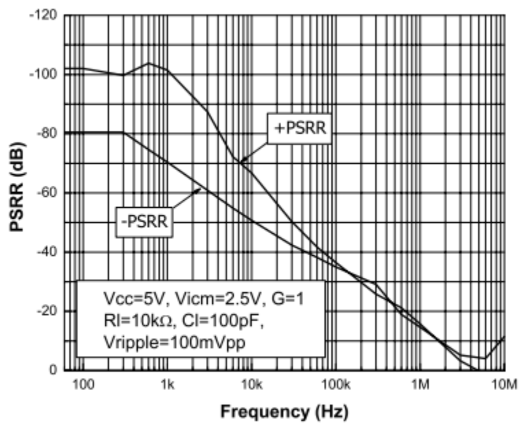


Figure 44. **PSSR vs. frequency**



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 SO8 package information

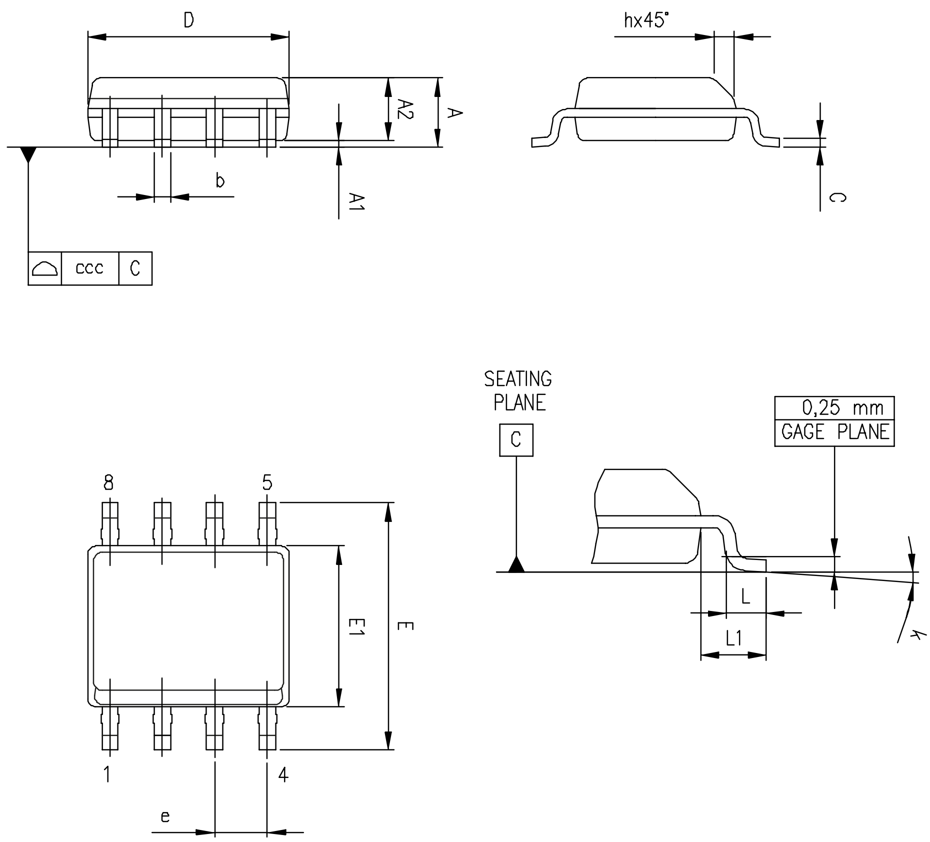


Figure 45. SO8 package outline

Table 6. SO8 mechanical data

Dim.	mm			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.1		0.25	0.004		0.01
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.01
D	4.8	4.9	5	0.189	0.193	0.197
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.9	4	0.15	0.154	0.157
e		1.27			0.05	
h	0.25		0.5	0.01		0.02
L	0.4		1.27	0.016		0.05
L1		1.04			0.04	
k	0		8 °	1 °		8 °
ccc			0.1			0.004

5.2 SOT23-5 package information

Figure 46. SOT23-5 package outline

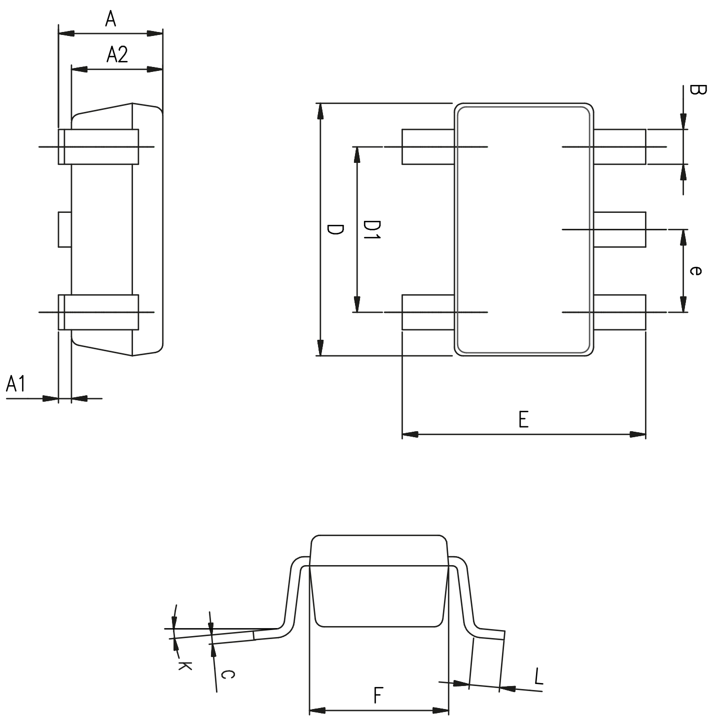


Table 7. SOT23-5 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

6 Ordering information

Table 8. **Order code**

Order code	Package	Packaging	Marking
TSZ181H1YLT [(1)]	SOT23-5	Tape & Reel	K230
TSZ182H1YDT [(1)]	SO8	Tape & Reel	Z182H1Y

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.*

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
01-Mar-2021	1	Initial release.
17-Jan-2023	2	Added new TSZ181H1YLT part number in Table 8. Order code and new SOT23-5 package information. Updated title, figure, features and description on the cover page. Updated Figure 1, Figure 3, Figure 4, Figure 5, Figure 6, Figure 7, Figure 8, Figure 9 and Figure 14.

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