

Description

The SiT5503 is a Stratum 3E MEMS precision oscillator optimized for ±5 ppb stability from -40°C to 95°C. Engineered for exceptional dynamic performance, it is ideal for replacing larger and less robust quartz OCXOs. SiT5503 is uniquely positioned for high reliability telecom, edge networking, IEEE 1588 PTP, and optical transport applications.

Leveraging SiTime’s unique DualMEMS® temperature sensing and TurboCompensation® technologies, the SiT5503 delivers the best dynamic performance for timing stability in the presence of environmental stressors such as air flow, temperature perturbation, vibration, shock, and electromagnetic interference. This device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for a dedicated external LDO.

The SiT5503 can be factory programmed for any combination of frequency, voltage, and pull range. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each frequency is custom built.

Refer to Manufacturing Guidelines for proper reflow profile and PCB cleaning recommendations to ensure best performance.

Features

- Any frequency from 1 MHz to 60 MHz in 1 Hz steps
- Factory programmable options for low lead time
- Best dynamic stability under airflow, thermal shock
 - ±5 ppb stability over temperature, -40°C to 95°C
 - ±0.3 ppb/°C typical frequency slope ($\Delta F/\Delta T$)
 - 2e-11 ADEV at 10 second averaging time
- No activity dips or micro jumps
- Resistant to shock, vibration and board bending
- On-chip regulators eliminate the need for external LDOs
- 2.5 V, 2.8 V, 3.0 V and 3.3 V supply voltage
- LVCMOS or clipped sinewave output
- RoHS and REACH compliant
- Pb-free, Halogen-free, Antimony-free
- 7.0 mm x 5.0 mm ceramic package
- [Contact SiTime](#) for tighter stability, wider temperature, and alternate package options

Applications

- 4G/5G radio, Small cell
- IEEE1588 boundary and grandmaster clocks
- Carrier-grade routers and switches
- Synchronous Ethernet
- Optical transport – SONET/SDH, OTN, Stratum 3E
- DOCSIS 3.x remote PHY
- GPS disciplined oscillators
- Precision GNSS systems
- Test and measurement



Block Diagram

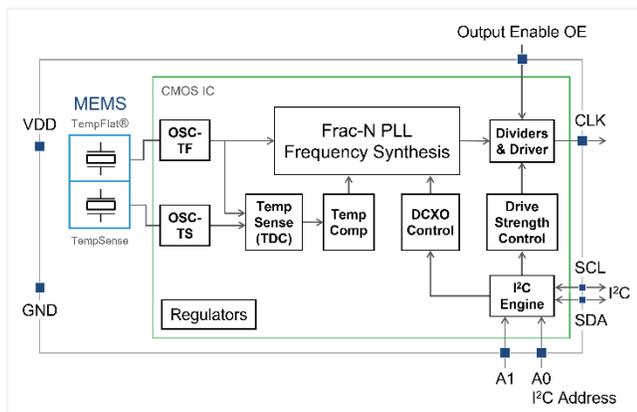


Figure 1. SiT5503 Block Diagram

7.0 mm x 5.0 mm Package Pinout

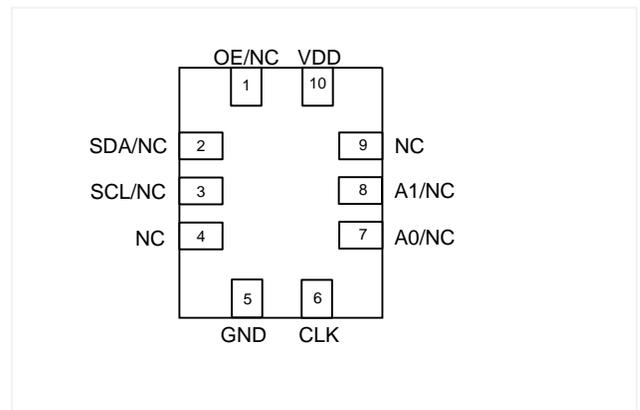
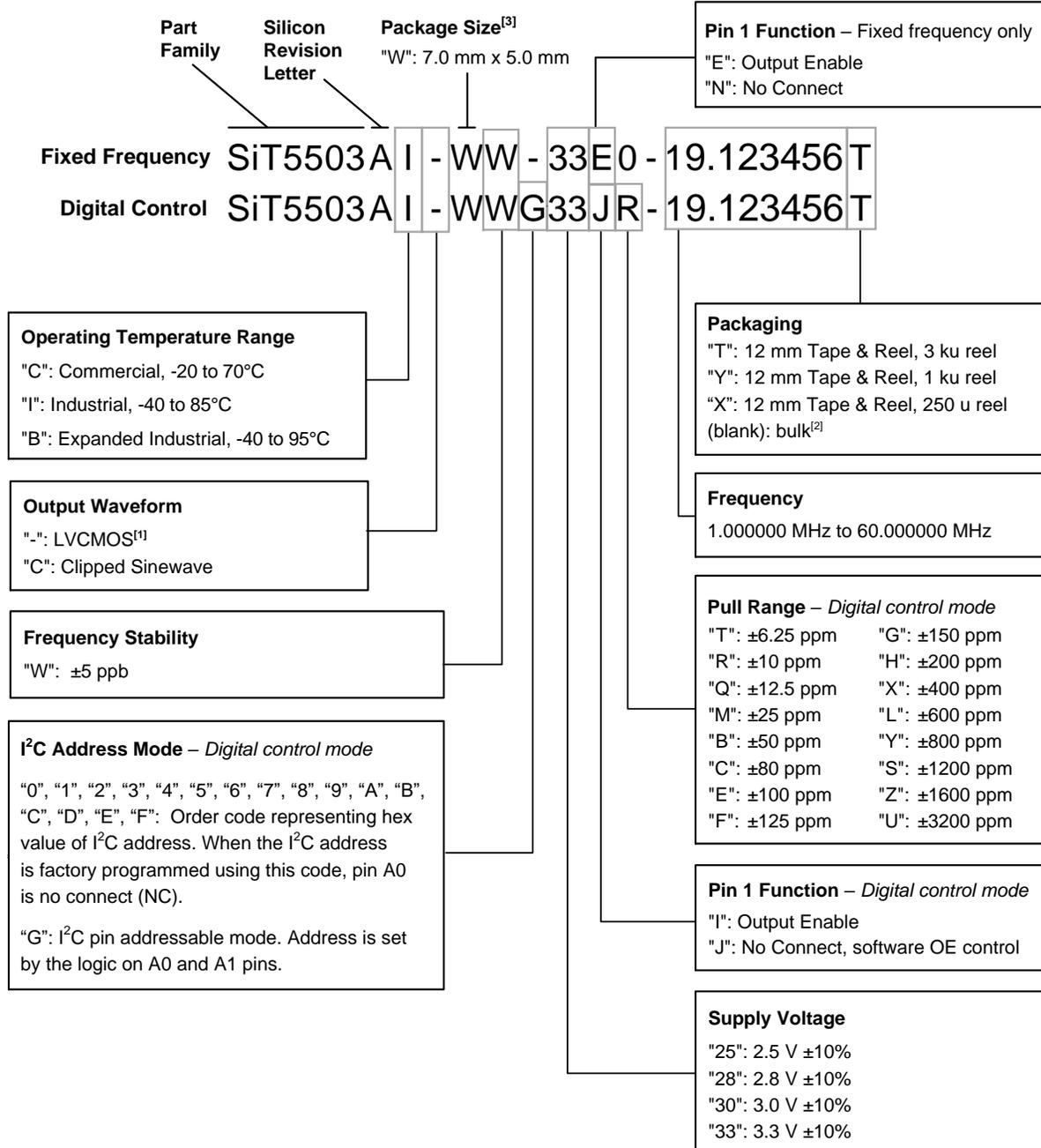


Figure 2. Pin Assignments (Top view)

Ordering Information

The part number guide illustrated below is for reference only, in which boxes identify order codes having more than one option. To customize and build an exact part number, use the SiTime [Part Number Generator](#). To validate the part number, use the SiTime [Part Number Decoder](#).



Notes:

- "-" corresponds to the default rise/fall time for LVCMOS output as specified in [Table 1](#) (Electrical Characteristics). [Contact SiTime](#) for other rise/fall time options for best EMI or driving multiple loads. For differential outputs, [contact SiTime](#).
- Bulk is available for sampling only.
- [Contact SiTime](#) for alternate package options.

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SiT5503 1 MHz – 60 MHz, Elite X™ ±5 ppb Precision Oscillator**Electrical Characteristics**

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and 3.3 V Vdd.

Table 1. Output Characteristics

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|--|-------------|------|--------|------|--------|--|
| Frequency Coverage | | | | | | |
| Nominal Output Frequency Range | F_nom | 1 | – | 60 | MHz | Contact SiTime for higher frequency options |
| Temperature Range | | | | | | |
| Operating Temperature Range | T_oper | -20 | – | +70 | °C | Commercial, ambient temperature |
| | | -40 | – | +85 | °C | Industrial, ambient temperature |
| | | -40 | – | +95 | °C | Expanded industrial, ambient temperature |
| Frequency Stability | | | | | | |
| Frequency Stability over Temperature | F_stab | -5 | – | +5 | ppb | Over operating temperature range (T_oper); referenced to (max frequency + min frequency)/2 over the temperature range. |
| Initial Tolerance | F_init | – | ±0.1 | – | ppm | Initial frequency at 25°C at 48 hours after 2 reflows |
| Supply Voltage Sensitivity | F_Vdd | – | ±1 | – | ppb | Over operating temperature range (T_oper); Vdd ±5% |
| Output Load Sensitivity | F_load | – | ±0.4 | – | ppb | Over operating temperature (T_oper); LVCMOS output, 15 pF ±10%. Clipped sinewave, 10 kΩ 10 pF ±10% |
| Frequency vs. Temperature Slope | ΔF/ΔT | – | ±0.3 | – | ppb/°C | 0.5°C/min temperature ramp rate, over operating temperature (T_oper) |
| Dynamic Frequency Change during Temperature Ramp | F_dynamic | – | ±0.003 | – | ppb/s | 0.5°C/min temperature ramp rate, over operating temperature (T_oper) |
| Hysteresis Over Temperature Contact SiTime for lower hysteresis | F_hys | – | ±1 | – | ppb | 0.5°C/min ramp rate, defined as ±ΔF/2, over operating temperature (T_oper) |
| One-Day Aging | F_1d | – | ±0.5 | – | ppb | At 85°C, after 30-days of continued operation. Aging is measured with respect to day 31 |
| One-Year Aging | F_1y | – | ±100 | – | ppb | At 85°C, after 2-days of continued operation. Aging is measured with respect to day 3 |
| 20-Year Aging | F_20y | – | ±300 | – | ppb | |
| 20-Year Total Stability | F_tot_20y | -4.6 | – | 4.6 | ppm | Complies with Stratum 3E per GR-1244-CORE. Actual performance is better |
| Allan deviation | ADEV | – | 2e-11 | – | – | 10 second averaging time ⁽⁴⁾ |
| LVCMOS Output Characteristics | | | | | | |
| Duty Cycle | DC | 45 | – | 55 | % | |
| Rise/Fall Time | Tr, Tf | 0.8 | 1.2 | 1.9 | ns | 10% - 90% Vdd |
| Output Voltage High | VOH | 90% | – | – | Vdd | IOH = +3 mA |
| Output Voltage Low | VOL | – | – | 10% | Vdd | IOL = -3 mA |
| Output Impedance | Z_out_c | – | 17 | – | Ohms | Impedance looking into output buffer, Vdd = 3.3 V |
| | | – | 17 | – | Ohms | Impedance looking into output buffer, Vdd = 3.0 V |
| | | – | 18 | – | Ohms | Impedance looking into output buffer, Vdd = 2.8 V |
| | | – | 19 | – | Ohms | Impedance looking into output buffer, Vdd = 2.5 V |
| Clipped Sinewave Output Characteristics | | | | | | |
| Output Voltage Swing | V_out | 0.8 | – | 1.2 | V | Clipped sinewave output, 10 kΩ 10 pF ±10% |
| Rise/Fall Time | Tr, Tf | – | 3.5 | 4.6 | ns | 20% - 80% Vdd, F_nom = 19.2 MHz |
| Start-up Characteristics | | | | | | |
| Start-up Time | T_start | – | 2.5 | 3.5 | ms | Time to first pulse, measured from the time Vdd reaches 90% of its final value. Vdd ramp time is 100 μs, 0 V to Vdd |
| Output Enable Time | T_oe | – | – | 680 | ns | F_nom = 10 MHz. See Timing Diagrams section below |
| Time to Rated Frequency Stability | T_stability | – | – | 1.6 | s | Time to first accurate pulse within rated stability, measured from the time Vdd reaches 90% of its final value. Vdd ramp time = 100 μs |

Note:

4. Measured 2 hours after startup in a temperature chamber with a constant temperature in still air.

SiT5503 1 MHz – 60 MHz, Elite X™ ±5 ppb Precision Oscillator

Table 2. DC Characteristics

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|-----------------|------|------|------|------|---|
| Supply Voltage | | | | | | |
| Supply Voltage | Vdd | 2.25 | 2.5 | 2.75 | V | Contact SiTime for 2.25 V to 3.63 V continuous supply voltage support |
| | | 2.52 | 2.8 | 3.08 | V | |
| | | 2.7 | 3.0 | 3.3 | V | |
| | | 2.97 | 3.3 | 3.63 | V | |
| Supply Voltage Ramp Time ^[5] | Vdd_rt | 150 | – | – | µs | Measured from power up to 100% of Vdd |
| Current Consumption | | | | | | |
| Current Consumption | I _{dd} | – | 44 | 53 | mA | F _{nom} = 19.2 MHz, No Load |
| OE Disable Current | I _{od} | – | 43 | 51 | mA | OE = GND, output weakly pulled down |

Table 3. Input Characteristics

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|-----------------|---|------|------|------|---------------------------|
| Input Characteristics – OE Pin | | | | | | |
| Input Impedance | Z _{in} | 75 | – | – | kΩ | Internal pull up to Vdd |
| Input High Voltage | V _{IH} | 70% | – | – | Vdd | |
| Input Low Voltage | V _{IL} | – | – | 30% | Vdd | |
| Frequency Tuning Range – I²C mode | | | | | | |
| Pull Range | PR | ±6.25 ±10 ±12.5 ±25 ±50 ±80 ±100 ±125 ±150 ±200 ±400 ±600 ±800 ±1200 ±1600 ±3200 | – | – | ppm | Digitally controlled mode |

Note:

5. SiT5503 requires a minimum supply voltage ramp time of 150 µs.

SiT5503 1 MHz – 60 MHz, Elite X™ ±5 ppb Precision Oscillator**Table 3. Input Characteristics – Continued**

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|--|------------------|--------|------|------|-----------------|---|
| Absolute Pull Range⁶⁾ | APR | ±5.85 | – | – | ppm | Over operating temperature range (T _{rated}); Digitally controlled mode for PR = ±6.25 ppm |
| I²C Interface Characteristics, 200 Ohm, 550 pF (Max I²C Bus Load) | | | | | | |
| Bus Speed | F _{I2C} | ≤ 400 | | | kHz | -40 to 95°C |
| | | ≤ 1000 | | | kHz | -40 to 85°C |
| Input Voltage Low | VIL_I2C | – | – | 30% | V _{dd} | Digitally controlled mode |
| Input Voltage High | VIH_I2C | 70% | – | – | V _{dd} | Digitally controlled mode |
| Output Voltage Low | VOL_I2C | – | – | 0.4 | V | Digitally controlled mode |
| Input Leakage current | I _L | 0.5 | – | 24 | μA | 0.1 V _{DD} < V _{OUT} < 0.9 V _{DD} . Includes typical leakage current from 200 kΩ pull resistor to VDD. Digitally controlled mode |
| Input Capacitance | C _{IN} | – | – | 5 | pF | Digitally controlled mode |

Note:

6. APR = PR – initial tolerance – 20-year aging – frequency stability over temperature.

Table 4. Phase Noise

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|-----------------------|--------|------|------|------|--------|--|
| Phase Noise | | | | | | |
| 1 Hz offset | | – | -73 | – | dBc/Hz | F _{nom} = 10 MHz Fixed frequency and digitally controlled mode with ±6.25 ppm pull range |
| 10 Hz offset | | – | -101 | – | dBc/Hz | |
| 100 Hz offset | | – | -122 | – | dBc/Hz | |
| 1 kHz offset | | – | -141 | – | dBc/Hz | |
| 10 kHz offset | | – | -149 | – | dBc/Hz | |
| 100 kHz offset | | – | -150 | – | dBc/Hz | |
| 1 MHz offset | | – | -161 | – | dBc/Hz | |

Device Configurations and Pin-outs

Table 5. Device Configurations

| Configuration | I ² C Programmable Parameters |
|----------------------|---|
| Fixed Frequency | – |
| Digitally Controlled | Frequency Pull Range, Frequency Pull Value, Output Enable control |

Pin-out Top Views

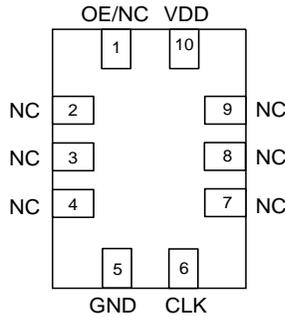


Figure 3. Fixed Frequency Device

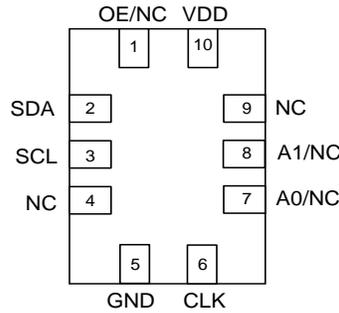


Figure 4. Digitally Controlled Device

Table 6. Pin Description

| Pin | Symbol | I/O | Internal Pull-up/Pull Down Resistor | Function |
|-----|-------------------------|--------------------------------|-------------------------------------|--|
| 1 | OE / NC ^[9] | OE – Input | 100 kΩ Pull-Up | H ^[7] : specified frequency output L: output is high impedance. Only output driver is disabled |
| | | NC ^[7] – No Connect | – | H or L or Open: No effect on output frequency or other device functions |
| 2 | SDA / NC ^[9] | SDA – Input/Output | 200 kΩ Pull Up | I ² C Serial Data |
| | | NC – No Connect | – | H or L or Open: No effect on output frequency or other device functions |
| 3 | SCL / NC ^[9] | SCL – Input | 200 kΩ Pull-Up | I ² C serial clock input |
| | | No Connect | – | H or L or Open: No effect on output frequency or other device functions |
| 4 | NC ^[9] | No Connect | – | H or L or Open: No effect on output frequency or other device functions |
| 5 | GND | Power | – | Connect to ground |
| 6 | CLK | Output | – | LVC MOS, or clipped sinewave oscillator output |
| 7 | A0/NC ^[9] | A0 – Input | 100 kΩ Pull-Up | For DCTCXO ordering code "G" only: I ² C Address Select, Least Significant Bit (LSB) <u>A1 A0 I²C Address</u> |
| 8 | A1/NC ^[9] | A1 – Input | 100 kΩ Pull-Up | 0 0 1100000 0 1 1100010 1 0 1101000 1 1 1101010 (Default) |
| 9 | NC ^[9] | No Connect | – | H or L or Open: No effect on output frequency or other device functions |
| 10 | VDD | Power | – | Connect to power supply ^[8] |

Notes:

- In OE mode for noisy environments, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
- A 0.1 μF capacitor in parallel with a 10 μF capacitor are required between VDD and GND. The 0.1 μF capacitor is recommended to place close to the device, and place the 10 μF capacitor less than 2 inches away.
- All NC pins can be left floating and do not need to be soldered down

Typical Performance Plots

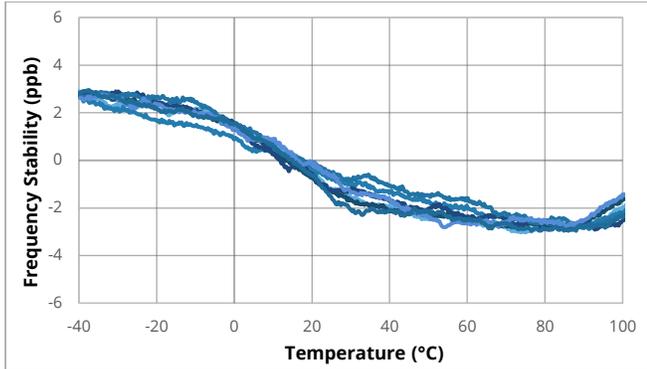


Figure 5. Frequency Stability

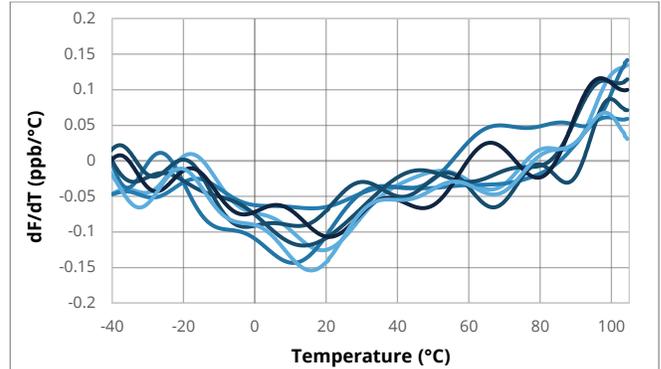


Figure 6. dF/dT

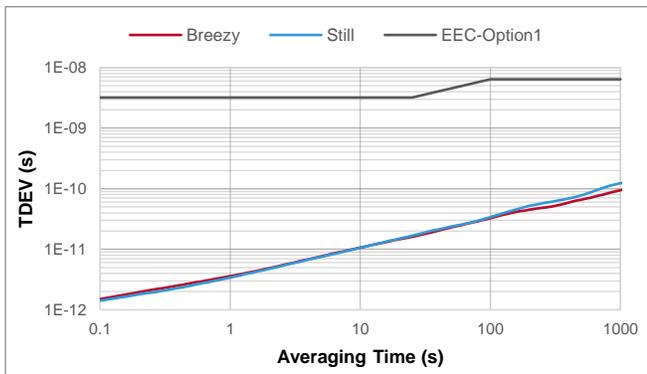


Figure 7. TDEV – Loop Bandwidth 3 Hz

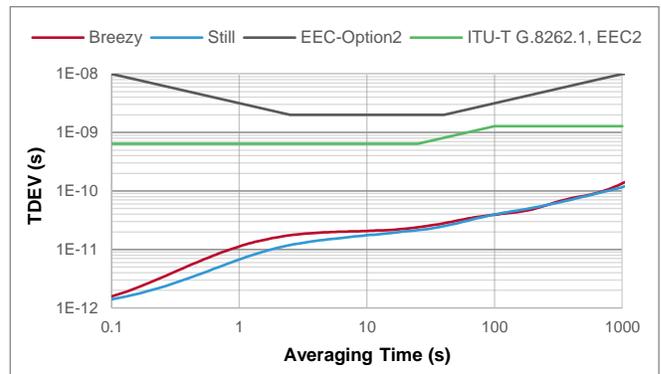


Figure 8. TDEV – Loop Bandwidth 0.1 Hz

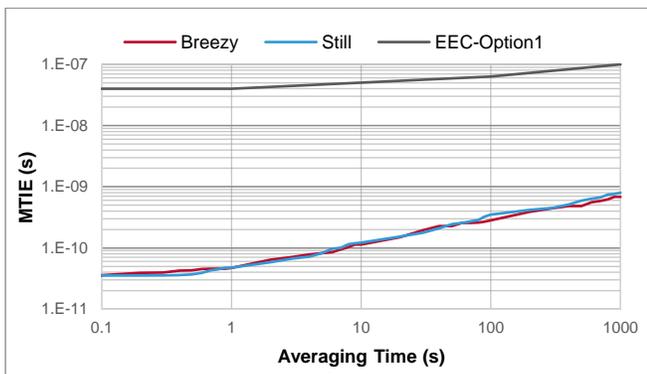


Figure 9. MTIE – Loop Bandwidth 3 Hz

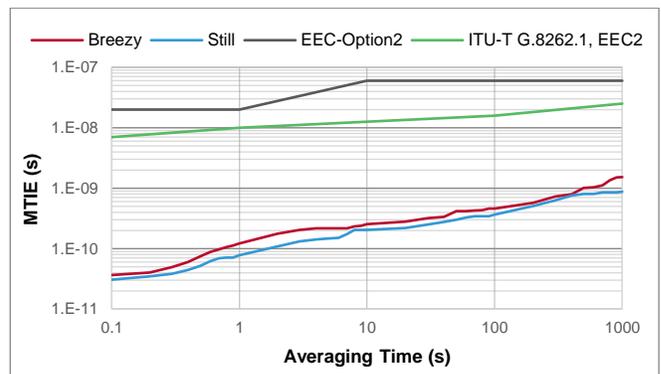


Figure 10. MTIE – Loop Bandwidth 0.1 Hz

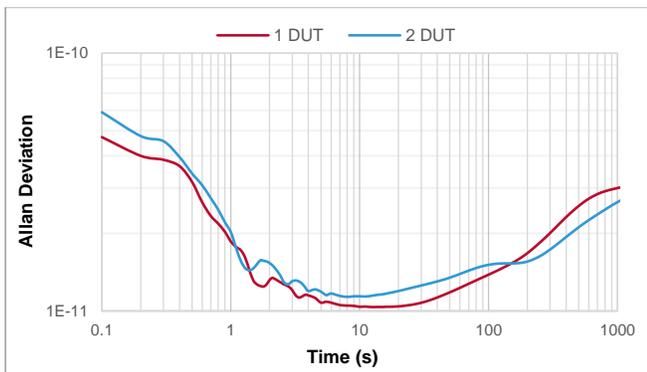


Figure 11. ADEV – Still Air

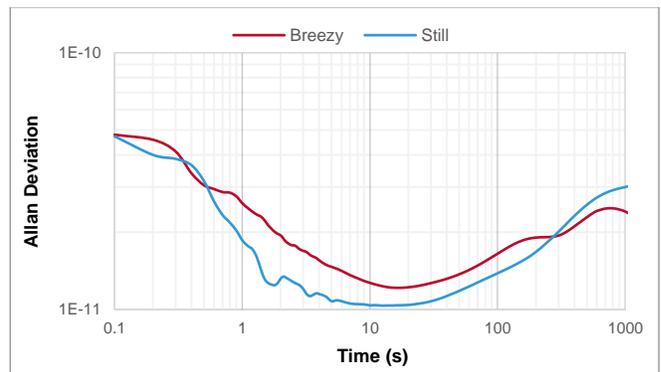
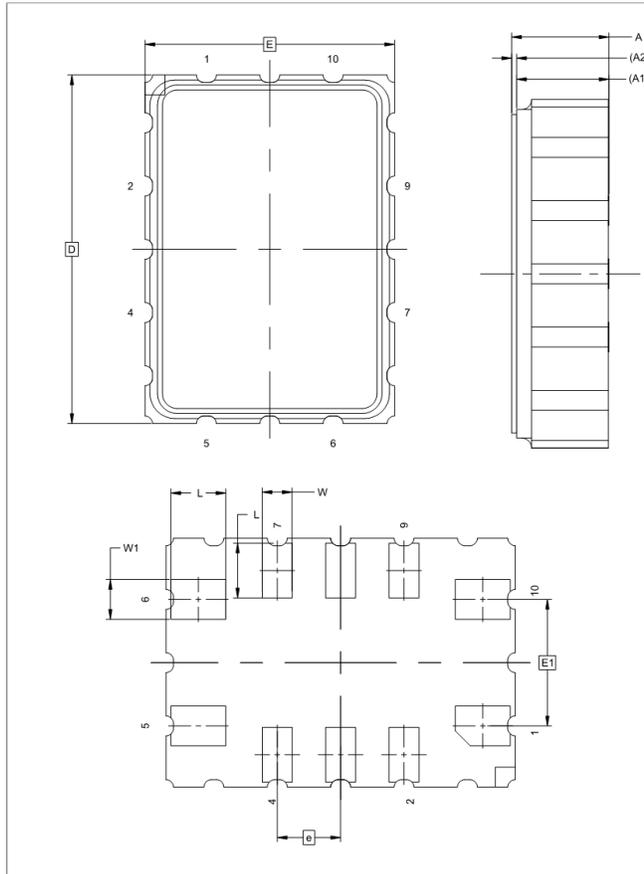


Figure 12. ADEV – Breezy Air

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)

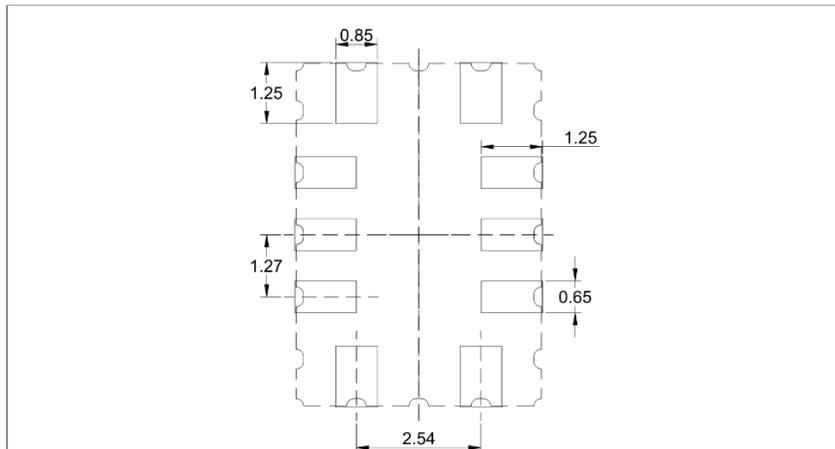


| | SYMBOL | MIN | NOM | MAX |
|------------------------|--------|-----------|-------|--------|
| TOTAL THICKNESS | A | | | 2.2000 |
| CERAMIC THICKNESS | A1 | 1.85 ref | | |
| LID THICKNESS | A2 | 0.100 ref | | |
| BODY SIZE | X | D 7 BSC | | |
| | Y | E 5 BSC | | |
| LEAD WIDTH | W | 0.550 | 0.600 | 0.650 |
| | W1 | 0.750 | 0.800 | 0.850 |
| LEAD LENGTH | L | 1.050 | 1.100 | 1.150 |
| LEAD PITCH | e | 1.27 BSC | | |
| | e1 | 2.54 BSC | | |
| PACKAGE EDGE TOLERANCE | aaa | 0.150 | | |
| COPLANARITY | ccc | 0.080 | | |

NOTE
1. ALL DIMENSION IN MM

| | | | |
|-------------------------------|-----------|------------------------|-------|
| | | | |
| PKG INFO | | DRAWING NO. | |
| 10L CQFN 7.000x5.00X2.2 mm | | POD-086-CQFN-010-X7050 | |
| DATE | 6/30/2021 | REV | SHEET |
| | | A00 | 01 |

Recommended Land Pattern (Unit: mm)



Note : All units in mm.

| | | | |
|--|--------------------|----------------------------|-------------------------|
| | PKG INFO | SPL DRAWING NO. | |
| | DATE 2021/06/16 | 10L CQFN 5.000x7.000 mm | SPL-086-CQFN-010-C07050 |
| | | REV | SHEET |
| | | Draft | 01 |

Revision History

Table 7. Revision History

| Version | Release Date | Change Summary |
|---------|--------------|---|
| 0.5 | 22-Sep-2022 | First release, preliminary information |
| 0.51 | 3-Nov-2022 | Resolved typographical error in the condition for the F_I2C specification |

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439

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Appendix

DCTCXO-Specific Design Considerations

Pull Range and Absolute Pull Range

Table 8 below shows the pull range and corresponding APR values for each of the frequency vs. temperature ordering options.

Table 8. APR Options^[10]

| Pull Range Ordering Code | Pull Range ppm | APR ppm ±5 ppb option |
|--------------------------|----------------|-----------------------|
| T | ±6.25 | ±5.85 |
| R | ±10 | ±9.59 |
| Q | ±12.5 | ±12.09 |
| M | ±25 | ±24.59 |
| B | ±50 | ±49.59 |
| C | ±80 | ±79.59 |
| E | ±100 | ±99.59 |
| F | ±125 | ±124.59 |
| G | ±150 | ±149.59 |
| H | ±200 | ±199.59 |
| X | ±400 | ±399.59 |
| L | ±600 | ±599.59 |
| Y | ±800 | ±799.59 |
| S | ±1200 | ±1199.59 |
| Z | ±1600 | ±1599.59 |
| U | ±3200 | ±3199.59 |

Notes:

10. APR includes initial tolerance, frequency stability vs. temperature, and the indicated 20-year aging.

Output Frequency

The device powers up at the nominal operating frequency and pull range specified by the ordering code. After power-up both pull range and output frequency can be controlled via I²C writes to the respective control registers. The maximum output frequency change is constrained by the pull range limits.

The pull range is specified by the value loaded in the digital pull-range control register. The 16 pull range choices are specified in the control register and range from ±6.25 ppm to ±3200 ppm.

Table 9 below shows the frequency resolution versus pull range programmed value

The ppm frequency offset is specified by the 26 bit DCXO frequency control register in two's complement format as described in the I²C Register Descriptions. The power up default value is 0000000000000000000000000000b which sets the output frequency at its nominal value (0 ppm). To change the output frequency, a frequency control word is written to 0x00[15:0] (Least Significant Word) and 0x01[9:0] (Most Significant Word). The LSW value should be written first followed by the MSW value; the frequency change is initiated after the MSW value is written.

Table 9. Frequency Resolution versus Pull Range

| Programmed Pull Range | Frequency Resolution |
|-----------------------|-----------------------|
| ±6.25 ppm | 5x10 ⁻¹² |
| ±10 ppm | 5x10 ⁻¹² |
| ±12.5 ppm | 5x10 ⁻¹² |
| ±25 ppm | 5x10 ⁻¹² |
| ±50 ppm | 5x10 ⁻¹² |
| ±80 ppm | 5x10 ⁻¹² |
| ±100 ppm | 5x10 ⁻¹² |
| ±120 ppm | 5x10 ⁻¹² |
| ±150 ppm | 5x10 ⁻¹² |
| ±200 ppm | 5x10 ⁻¹² |
| ±400 ppm | 1x10 ⁻¹¹ |
| ±600 ppm | 1.4x10 ⁻¹¹ |
| ±800 ppm | 2.1x10 ⁻¹¹ |
| ±1200 ppm | 3.2x10 ⁻¹¹ |
| ±1600 ppm | 4.7x10 ⁻¹¹ |
| ±3200 ppm | 9.4x10 ⁻¹¹ |

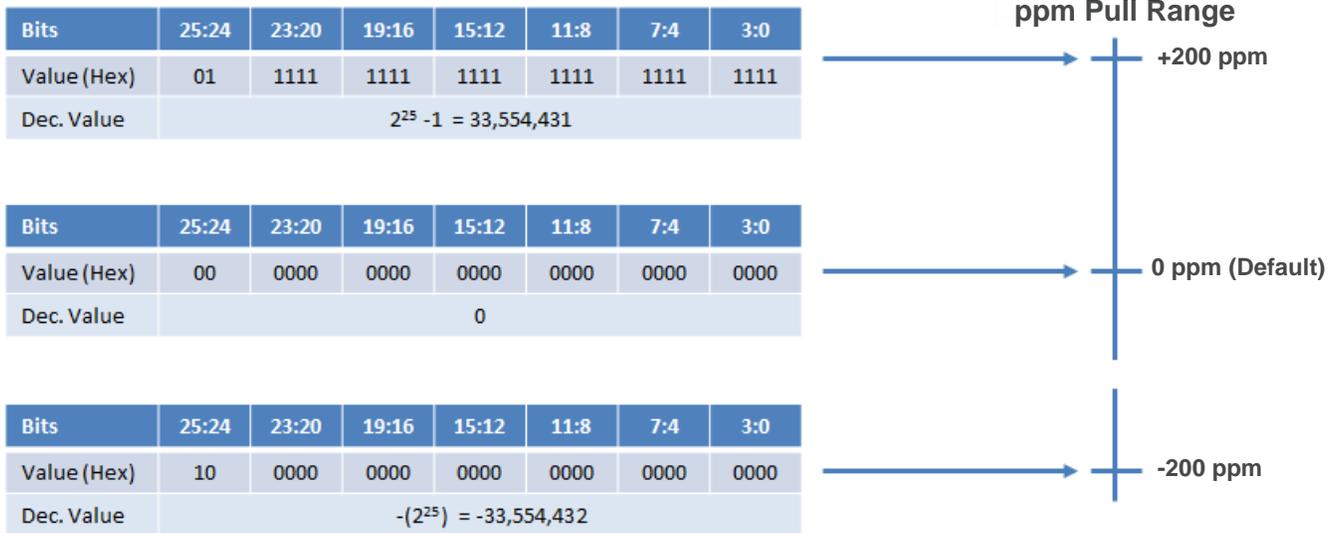


Figure 14. Pull Range and Frequency Control Word

Figure 14 shows how the two's complement signed value of the frequency control word sets the output frequency within the ppm pull range set by 0x02:[3:0]. This example shows use of the ±200 ppm pull range. Therefore, to set the desired output frequency, one just needs to calculate the fraction of full scale value ppm, convert to two's complement binary, and then write these values to the frequency control registers.

The following formula generates the control word value:

Control word value = RND($2^{25}-1$) × ppm shift from nominal/pull range), where RND is the rounding function which rounds the number to the nearest whole number. Two examples follow, assuming a ±200 ppm pull range:

Example 1:

- Default Output Frequency = 19.2 MHz
- Desired Output Frequency = 19.201728 MHz (+90 ppm)

$2^{25}-1$ corresponds to +200 ppm, and the fractional value required for +90 ppm can be calculated as follows.

- $90 \text{ ppm} / 200 \text{ ppm} \times (2^{25}-1) = 15,099,493.95.$

Rounding to the nearest whole number yields 15,099,494 and converting to two's complement gives a binary value of 111001100110011001100110, or E66666 in hex.

Example 2:

- Default Output Frequency = 10 MHz
- Desired Output Frequency = 9.9995 MHz (-50 ppm)

Following the formula shown above,

- $(-50 \text{ ppm} / 200 \text{ ppm}) \times (2^{25}) = -8,388,608.$

Converting this to two's complement binary results in 111000000000000000000000, or 3800000 in hex.

To summarize, the procedure for calculating the frequency control word associated with a given ppm offset is as follows:

- 1) Calculate the fraction of the half-pull range needed. For example, if the total pull range is set for ±100 ppm and a +20 ppm shift from the nominal frequency is needed, this fraction is 20 ppm/100 ppm = 0.2
- 2) Multiply this fraction by the full-half scale word value, $2^{25}-1 = 33,554,431$, round to the nearest whole number, and convert the result to two's complement binary. Following the +20 ppm example, this value is $0.2 \times 33,554,431 = 6,710,886.2$ and rounded to 6,710,886.
- 3) Write the two's complement binary value starting with the Least Significant Word (LSW) 0x00[16:0], followed by the Most Significant Word (MSW), 0x01[9:0]. If the user desires that the output remains enabled while changing the frequency, a 1 must also be written to the OE control bit 0x01[10] if the device has software OE Control Enabled.

It is important to note that the maximum Digital Control update rate is 38 kHz regardless of I²C bus speed.

I²C Control Registers

The SiT5503 enables control of frequency pull range, frequency pull value, and Output Enable via I²C writes to the control registers. Table 10 below shows the register map summary, and detailed register descriptions follow.

Table 10. Register Map Summary

| Address | Bits | Access | Description |
|---------|---------|--------|--|
| 0x00 | [15:0] | RW | DIGITAL FREQUENCY CONTROL LEAST SIGNIFICANT WORD (LSW) |
| 0x01 | [15:11] | R | NOT USED |
| | [10] | RW | OE Control. This bit is only active if the output enable function is under software control. If the device is configured for hardware control using the OE pin, writing to this bit has no effect. |
| | [9:0] | RW | DIGITAL FREQUENCY CONTROL MOST SIGNIFICANT WORD (MSW) |
| 0x02 | [15:4] | R | NOT USED |
| | [3:0] | RW | DIGITAL PULL RANGE CONTROL |

Register Descriptions

Register Address: 0x00. Digital Frequency Control Least Significant Word (LSW)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Name | DIGITAL FREQUENCY CONTROL LEAST SIGNIFICANT WORD (LSW)[15:0] | | | | | | | | | | | | | | | |

| Bits | Name | Access | Description |
|------|--|--------|--|
| 15:0 | DIGITAL FREQUENCY CONTROL LEAST SIGNIFICANT WORD | RW | <p>Bits [15:0] are the lower 16 bits of the 26 bit FrequencyControlWord and are the Least Significant Word (LSW). The upper 10 bits are in register 0x01[9:0] and are the Most Significant Word (MSW). The lower 16 bits together with the upper 10 bits specify a 26-bit frequency control word.</p> <p>This power-up default values of all 26 bits are 0 which sets the output frequency at its nominal value. After power-up, the system can write to these two registers to pull the frequency across the pull range. The register values are two's complement to support positive and negative control values. The LSW value should be written before the MSW value because the frequency change is initiated when the new values are loaded into the MSW. More details and examples are discussed in the previous section.</p> |

Register Address: 0x01. OE Control, Digital Frequency Control Most Significant Word (MSW)

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------|----|----|----|----|----|---------------------------------|----|----|----|----|----|----|----|----|----|
| Access | R | R | R | R | R | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Name | NOT USED | | | | | OE | DCXO FREQUENCY CONTROL[9:0] MSW | | | | | | | | | |

| Bits | Name | Access | Description |
|-------|---|--------|---|
| 15:11 | NOT USED | R | Bits [15:10] are read only and return all 0's when read. Writing to these bits has no effect. |
| 10 | OE Control | RW | Output Enable Software Control. Allows the user to enable and disable the output driver via I ² C. 0 = Output Disabled (Default) 1 = Output Enabled This bit is only active if the Output Enable function is under software control. If the device is configured for hardware control using the OE pin, writing to this bit has no effect. |
| 9:0 | DIGITAL FREQUENCY CONTROL MOST SIGNIFICANT WORD (MSW) | RW | Bits [9:0] are the upper 10 bits of the 26 bit FrequencyControlWord and are the Most Significant Word (MSW). The lower 16 bits are in register 0x00[15:0] and are the Least Significant Word (LSW). These lower 16 bits together with the upper 10 bits specify a 26-bit frequency control word. This power-up default values of all 26 bits are 0 which sets the output frequency at its nominal value. After power-up, the system can write to these two registers to pull the frequency across the pull range. The register values are two's complement to support positive and negative control values. The LSW value should be written before the MSW value because the frequency change is initiated when the new values are loaded into the MSW. More details and examples are discussed in the previous section. |

Register Address: 0x02. DIGITAL PULL RANGE CONTROL^[11]

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|------|----|----|----|----|----|---|---|---|---|---|---|----------------------------|----|----|----|
| Access | R | R | R | R | R | R | R | R | R | R | R | R | RW | RW | RW | RW |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | X | X | X | X |
| Name | NONE | | | | | | | | | | | | DIGITAL PULL RANGE CONTROL | | | |

Notes:

11. Default values are factory set but can be over-written after power-up.

| Bits | Name | Access | Description |
|------|----------------------------|--------|--|
| 15:4 | NONE | R | Bits [15:4] are read only and return all 0's when read. Writing to these bits has no effect. |
| 3:0 | DIGITAL PULL RANGE CONTROL | RW | <p>Sets the digital pull range of the DCXO. The table below shows the available pull range values and associated bit settings. The default value is factory programmed.</p> <p>Bit</p> <p>3 2 1 0</p> <p>0 0 0 0: ±6.25 ppm</p> <p>0 0 0 1: ±10 ppm</p> <p>0 0 1 0: ±12.5 ppm</p> <p>0 0 1 1: ±25 ppm</p> <p>0 1 0 0: ±50 ppm</p> <p>0 1 0 1: ±80 ppm</p> <p>0 1 1 0: ±100 ppm</p> <p>0 1 1 1: ±125 ppm</p> <p>1 0 0 0: ±150 ppm</p> <p>1 0 0 1: ±200 ppm</p> <p>1 0 1 0: ±400 ppm</p> <p>1 0 1 1: ±600 ppm</p> <p>1 1 0 0: ±800 ppm</p> <p>1 1 0 1: ±1200 ppm</p> <p>1 1 1 0: ±1600 ppm</p> <p>1 1 1 1: ±3200 ppm</p> |

Serial Interface Configuration Description

The SiT5503 includes an I²C interface to access registers that control the DCTCXO frequency pull range, and frequency pull value. The SiT5503 I²C slave-only interface supports clock speeds up to 1 Mbit/s. The SiT5503 I²C module is based on the I²C specification, UM1024 (Rev.6 April 4, 2014 of NXP Semiconductor).

Serial Signal Format

The SDA line must be stable during the high period of the SCL. SDA transitions are allowed only during SCL low level for data communication. Only one transition is allowed during the low SCL state to communicate one bit of data. [Figure 15](#) shows the detailed timing diagram.

An idle I²C bus state occurs when both SCL and SDA are not being driven by any master and are therefore in a logic HI state due to the pull up resistors. Every transaction begins with a START (S) signal and ends with a STOP (P) signal. A START condition is defined by a high to low transition on the SDA while SCL is high. A STOP condition is defined by a low to high transition on the SDA while SCL is high. START and STOP conditions are always generated by the master. This slave module also supports repeated START (Sr) condition which is same as START condition instead of STOP condition (the blue-color line shows repeated START in [Figure 16](#)).

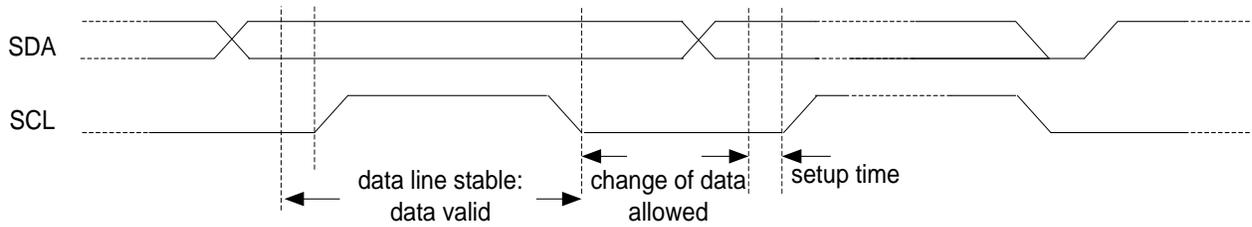


Figure 15. Data and clock timing relation in I²C bus

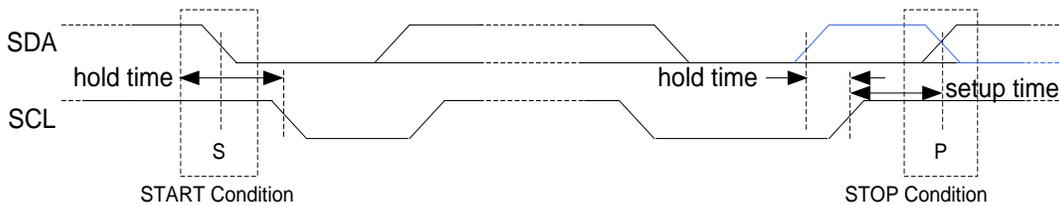


Figure 16. START and STOP (or repeated START, blue line) condition

Parallel Signal Format

Every data byte is 8 bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the MSB (Most Significant Bit) first. The detailed data transfer format is shown in Figure 18 below.

The acknowledge bit must occur after every byte transfer and it allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. The acknowledge signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low and it remains stable low during the high period of this clock pulse. Setup and hold times must also be taken into account. When SDA remains high during this ninth clock pulse, this is defined as the Not-Acknowledge signal (NACK). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer. The only condition that leads to the generation of NACK from the SiT5503 is when the transmitted address does not match the slave address. When the master is reading data from the SiT5503, the SiT5503 expects the ACK from the master at the end of received data, so that the slave releases the SDA line and the master can generate the STOP or repeated START. If there is a NACK signal at the end of the data, then the SiT5503 tries to send the next data. If the first bit of the next data is “0”, then the SiT5503 holds the SDA line to “0”, thereby blocking the master from generating a STOP/(re)START signal.

Parallel Data Format

This I²C slave module supports 7-bit device addressing format. The 8th bit is a read/write bit and “1” indicates a read transaction and a “0” indicates a write transaction. The register addresses are 8-bits long with an address range of 0 to 255 (00h to FFh). Auto address incrementing is supported which allows data to be transferred to contiguous addresses without the need to write each address beyond the first address. Since the maximum register address value is 255, the address will roll from 255 back to 0 when auto address incrementing is used. Obviously, auto address incrementing should only be used for writing to contiguous addresses. The data format is 16-bit (two bytes) with the most significant byte being transferred first. For a read operation, the starting register address must be written first. If that is omitted, reading will start from the last address in the auto-increment counter of the device, which has a startup default of 0x00.

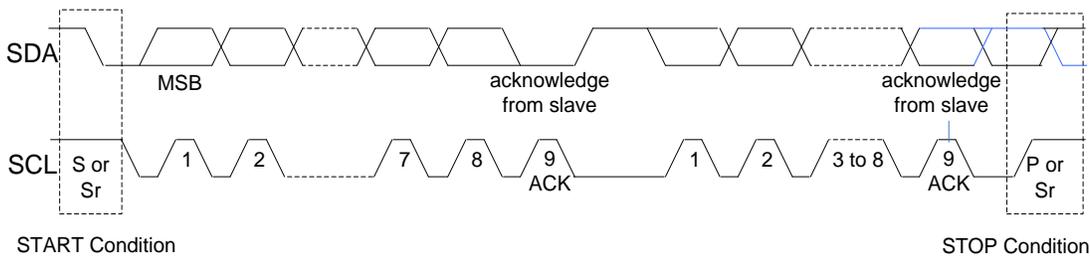


Figure 17. Parallel signaling format

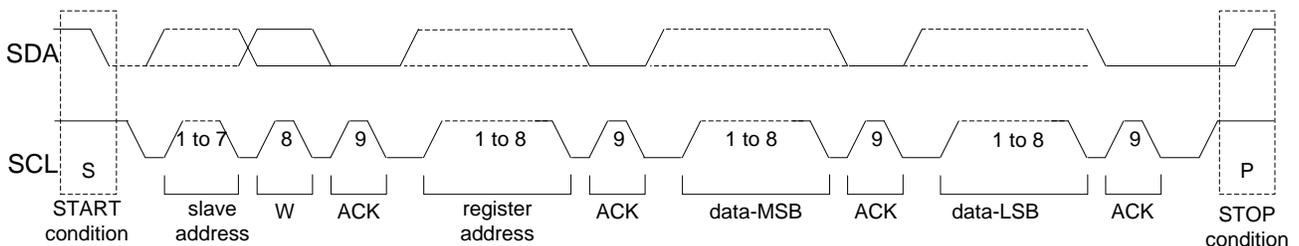


Figure 18. Parallel data byte format, write operation

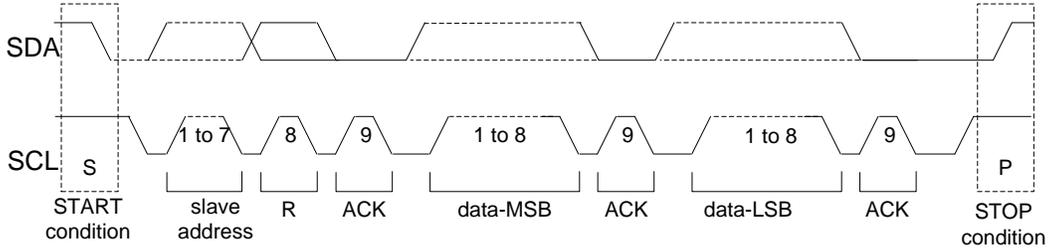


Figure 19. Parallel data byte format, read operation

Figure 20 below shows the I²C sequence for writing the 4-byte control word using auto address incrementing.

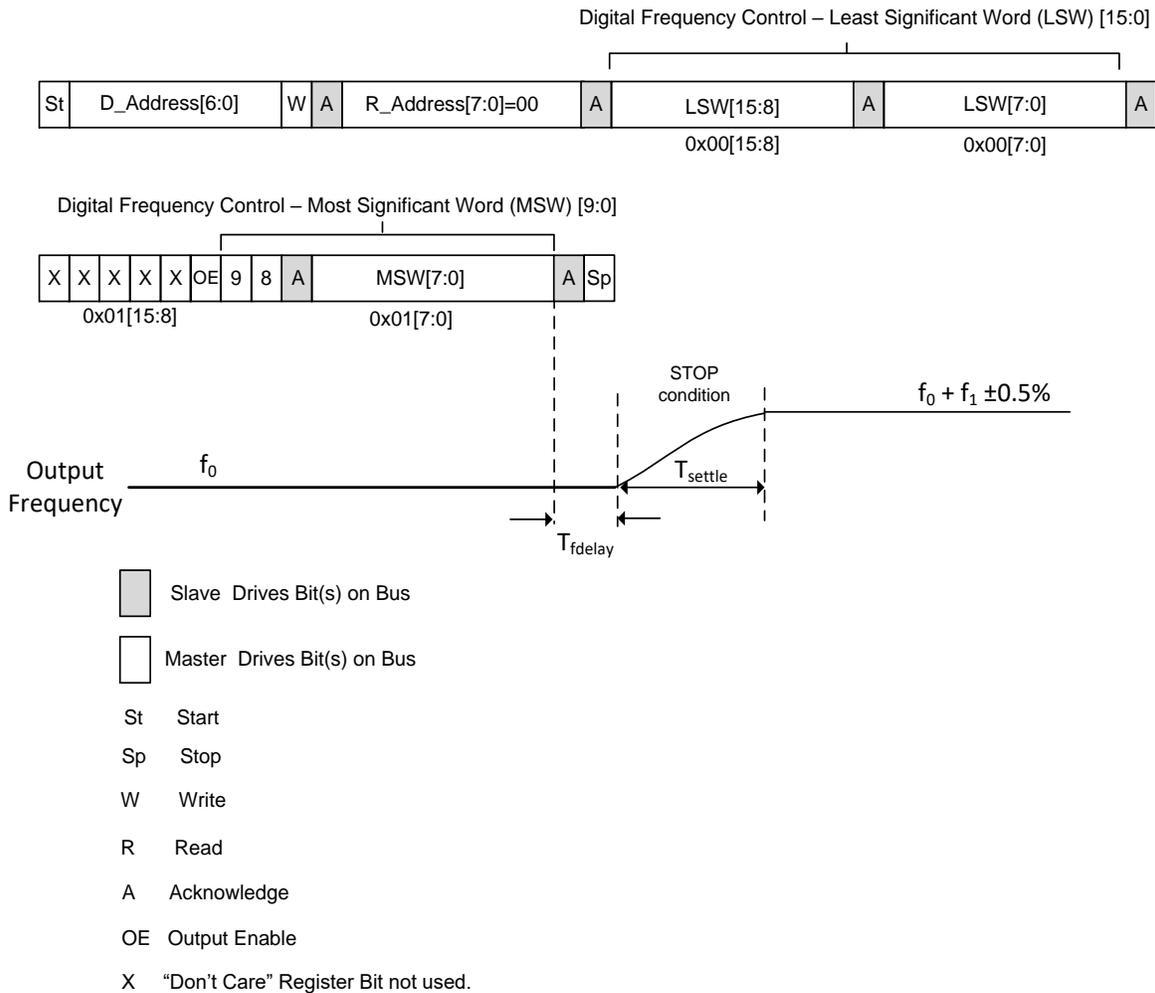


Figure 20. Writing the Frequency Control Word

Table 11. DCTCXO Delay and Settling Time

| Parameter | Symbol | Minimum | Typical | Maximum | Units | Notes |
|-------------------------|--------------|---------|---------|---------|---------|---|
| Frequency Change Delay | T_{fdelay} | – | 103 | 140 | μs | Time from end of 0x01 reg MSW to start of frequency pull, as shown in Figure 20 |
| Frequency Settling Time | T_{settle} | – | 16.5 | 20 | μs | Time to settle to 0.5% of frequency offset, as shown in Figure 20 |

I²C Timing Specification

The below timing diagram and table illustrate the timing relationships for both master and slave.

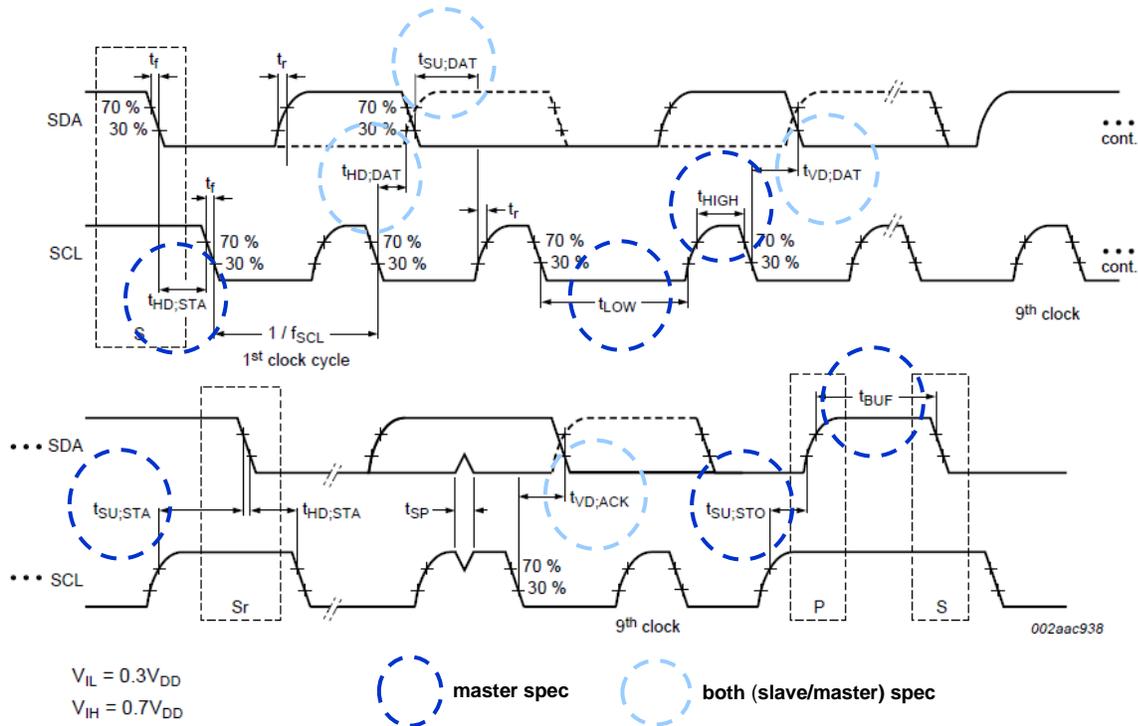


Figure 21. I²C Timing Diagram

Table 12. I²C Timing Requirements

| Parameter | Speed Mode | Value | Unit |
|--------------|--------------|------------------------------------|------|
| t_{SETUP} | FM+ (1 MHz) | > 50 | nsec |
| | FM (400 KHz) | > 100 | nsec |
| | SM (100 KHz) | > 250 | nsec |
| t_{HOLD} | FM+ (1 MHz) | > 0 | nsec |
| | FM (400 KHz) | > 0 | nsec |
| | SM (100 KHz) | > 0 | nsec |
| $t_{VD:AWK}$ | FM+ | > 450 | nsec |
| | FM (400 KHz) | > 900 | nsec |
| | SM (100 KHz) | > 3450 | nsec |
| $t_{VD:DAT}$ | | NA (s-awk + s-data)/(m-awk/s-data) | |

I²C Device Address Modes

There are two I²C address modes:

- 4) Factory Programmed Mode. The lower 4 bits of the 7-bit device address are set by ordering code as shown in [Table 13](#) below. There are 16 factory programmed addresses available. In this mode, pin 5 is NC and the A0 I²C address pin control function is not available.
- 5) A0 Pin Control. This mode allows the user to select between two I²C Device addresses as shown in [Table 14](#).

Table 13. Factory Programmed I²C Address Control^[12]

| I ² C Address Ordering Code | Device I ² C Address |
|--|---------------------------------|
| 0 | 1100000 |
| 1 | 1100001 |
| 2 | 1100010 |
| 3 | 1100011 |
| 4 | 1100100 |
| 5 | 1100101 |
| 6 | 1100110 |
| 7 | 1100111 |
| 8 | 1101000 |
| 9 | 1101001 |
| A | 1101010 |
| B | 1101011 |
| C | 1101100 |
| D | 1101101 |
| E | 1101110 |
| F | 1101111 |

Notes:

12. [Table 13](#) is only valid for the DCTCXO device option which supports I²C Control.

Table 14. Pin Selectable I²C Address Control^[13]

| A0 Pin 7 | A1 Pin 8 | I ² C Address |
|-------------|-------------|--------------------------|
| 0 | 0 | 1100000 |
| 0 | 1 | 1100010 |
| 1 | 0 | 1101000 |
| 1 | 1 | 1101010 (Default) |

Notes:

13. [Table 14](#) is only valid for the DCTCXO device option which supports I²C control with A0 and A1 Device Address Control Pins.

Schematic Example

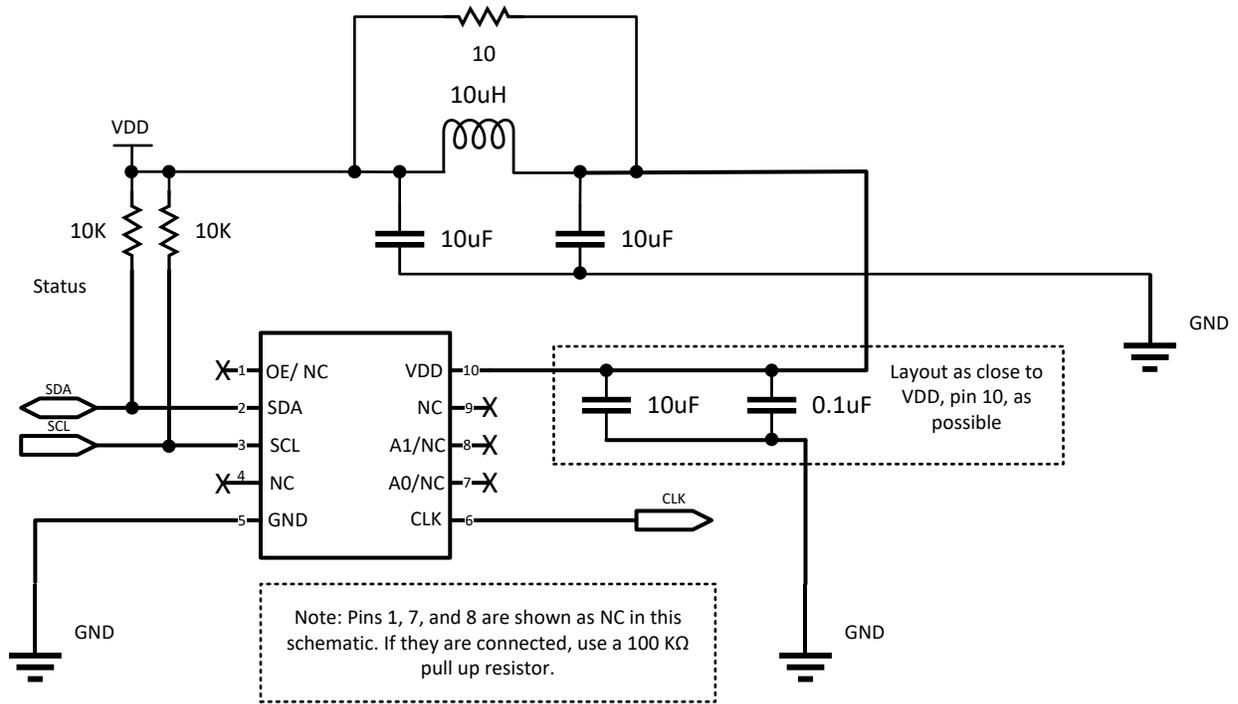


Figure 22. DCTCXO schematic example