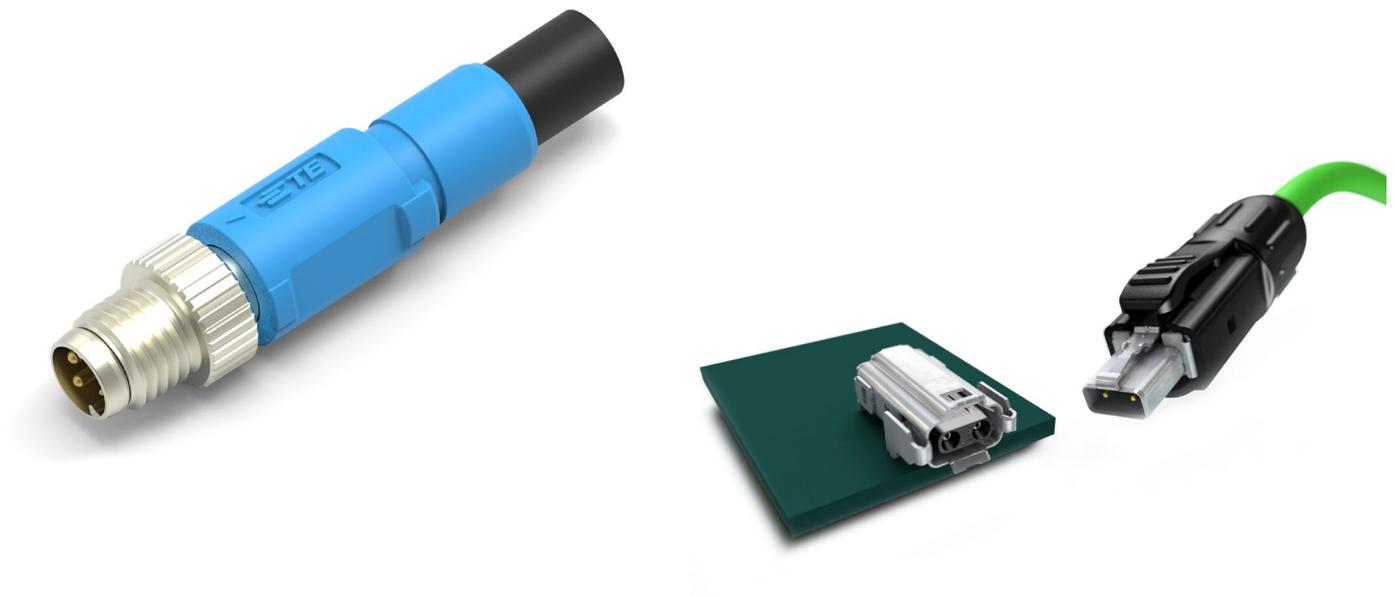


# Higher Power Levels for Single Pair Ethernet

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## Summary

An SPE connector is introduced that is designed for industrial environments with two pin pairs where one is used for data transmission up to 1Gbps/600MHz and the other one supports power transmission with currents up to 8A. This hybrid connector with a data and power pin pair features a metal shield separating the pin pairs to avoid the interference of the power signal with the data signal. Therefore, it gains more flexibility regarding increased power levels and flexibility on network topologies for the power lines. This all is placed within the form factor of an M8 connector what leads to the challenge of avoiding the deterioration of the data transmission by higher harmonics from the power transmission, like from switch mode power supplies.

## Introduction

Single-Pair Ethernet (SPE) provides data transmission up to 1Gbps over a single twisted copper pair. By the reduction from the four or eight wires of the traditional Fast Ethernet and Gigabit Ethernet towards two wires, this technology enables smaller connector sizes and decreases the termination effort. It is thus suitable to bring Ethernet down to the sensor level and to connect sensors directly to IT systems (aka the cloud) to support the added-value services of the Industrial Internet of Things (IIoT).

The first SPE implementations are supposed to extend existing automation systems by additional sensors to provide machine data to higher level IT (cloud) systems in order to enable added-value IIoT services such as condition monitoring and predictive maintenance. Such implementations will use a hierarchical star structure where the power for the I/O modules and sensors at the lower level needs to be delivered over the same cable used for data transmission. For the 40m/1Gbps segment that targets Factory Automation applications, Power over Data Line (PoDL) [1] is suitable for currents up to 1.36A. However, for higher currents which often occur in such a cascaded structure, a different approach is required.

An SPE connector design for industrial environments with two pin pairs has been recently developed where one is used for data transmission up to 1Gbps/600MHz as defined by IEEE 802.3bp [2] and the other one supports power transmission with currents up to 8A. This connector's interface is standardized in IEC 63171-6 [3] together with a variant without an extra power pair, which was published on the 20th of January 2020. Connectors with the two interface variants included in this standard are shown in Figure 1. The hybrid connector with a data and power pin pair features a metal shield separating the pin pairs to avoid the interference of the power signal with the data signal as can be seen in Figure 2. This all is placed within the form factor of an M8 connector what leads to the challenge of avoiding the deterioration of the data transmission by higher harmonics from the power transmission, like from switch mode power supplies. This connector requires a cable that contains an SPE and a power pair. In this cable the SPE pair is designed according to IEC 61156-12 and this SPE pair is also shielded from the power pair like in the connector. The power pair is made of 18AWG wires.



Figure 1: Single Pair Ethernet connectors per IEC 63171-6: (a) IP20 connector for SPE where power may be delivered via PoDL with max. 1,36 A (b) IP67 hybrid connector for SPE with separate power contacts allowing for currents up to 8 A

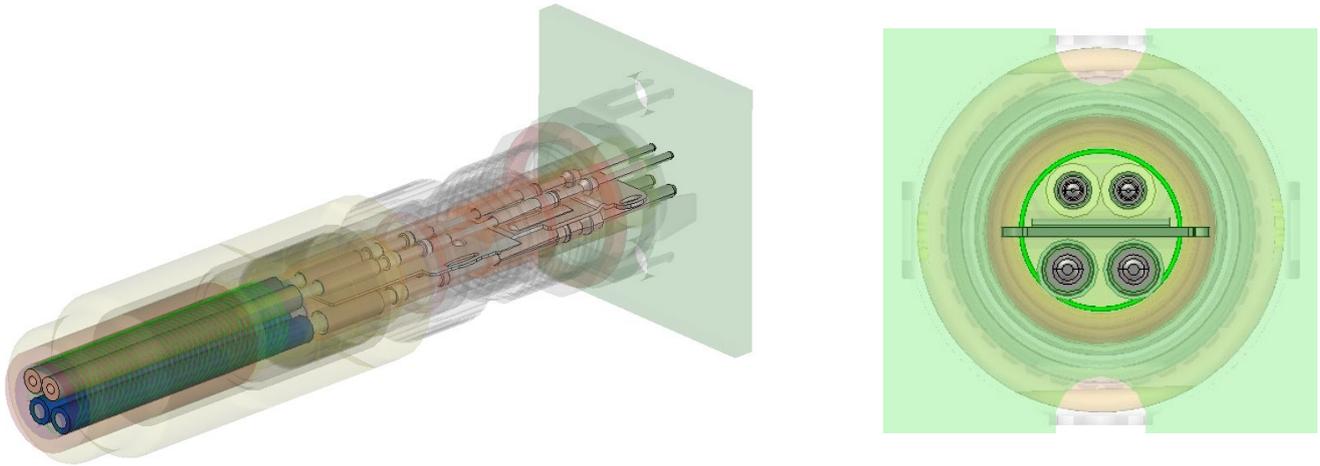


Figure 2: Internal shielding of IP67 connector avoiding interferences from the power lines to the data lines: (a) Perspective view, (b) Cross-section view

### PoDL or separate power lines

PoDL is a very compact way to combine power and data on only two signal wires what has been standardized in IEEE802.3bu. It enables a lot of new future applications requiring smaller and lighter connectivity solutions. At the moment PoDL is defined for a point to point connection that on one side has the power supply, named “Power Sourcing Equipment” (PSE) within IEEE, and on the other side the “Powered Device” (PD). When the power is injected on or tapped off the data line it should not disturb the data transmission. A typical circuitry that could be used to connect the PHY chip and the power to the data lines is shown in Figure 3. The basic circuitry of SPE requires a common mode choke (CMC) combined with common mode terminations to suppress common mode noise, and DC block capacitors. The power lines can be connected to the SPE lines by adding a low pass filter or only series inductors in between the PSE or the PD and the data lines to not disturb the data signals.

There are situations where it may become important to deviate from the PoDL standard. Reasons for this can be diverse, like the need for higher power levels, e.g. required for the supply of electronic motors. Also, more flexibility regarding how to distribute the power over the network to provide power to several cascaded PDs can be important. Another possible reason for avoiding PoDL is the need for a galvanic separation between data and power. This could for example reduce the effort of filtering of the power signals. Therefore, the hybrid connector is developed that has separate signal and power pairs, but still offers one connectivity solution for data and power in the small form factor of standard M8 connectors. The power contacts can handle a current of 8A. Below sections detail the possibilities of such a hybrid connector are discussed.

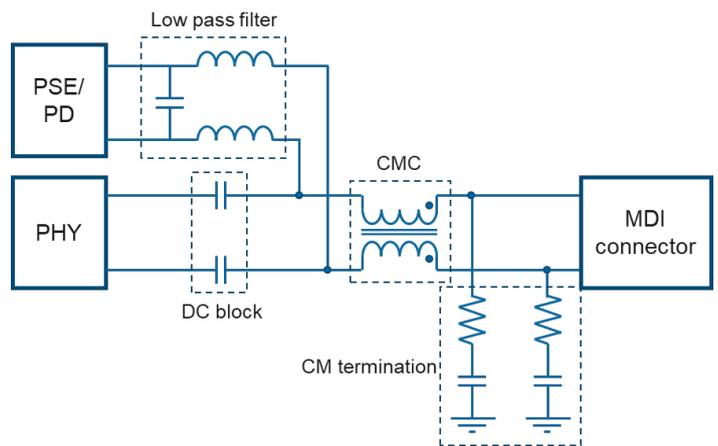


Figure 3: Generic SPE circuitry with PoDL

## Power transfer

With PoDL the highest power level that can be delivered to the PD is about 50W with a maximum current of 1.36A. This also requires the highest voltage from the PSE side of 60VDC (resulting in min. 48VDC at the PD). The higher current-carrying capabilities of the hybrid connector provide the opportunity of supplying higher power levels. In the end the received power levels depends on the permitted voltage drop and the acceptable amount of losses over the cable. To obtain insight in the possible power transfers we assume the basic setup as described in [4] that is shown in Figure 4.

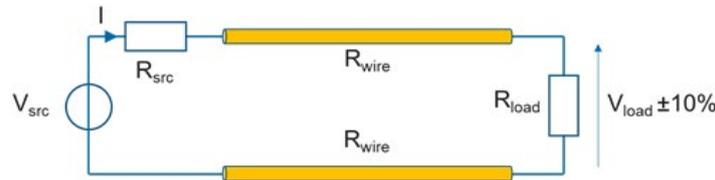


Figure 4: Basic circuitry for power transfer

Figure 4 shows the Power Sourcing Equipment (PSE) on the left that includes here a voltage source with an internal resistance. The second part is the cable with losses and on the right, we have the Powered Device (PD) that contains a load resistance that requires a specific voltage range. With this setup we can determine the power and current transferred over a defined length of cable. If we assume an 18AWG copper wire and for simplification neglect the source resistance we obtain the results given in Figure 5.

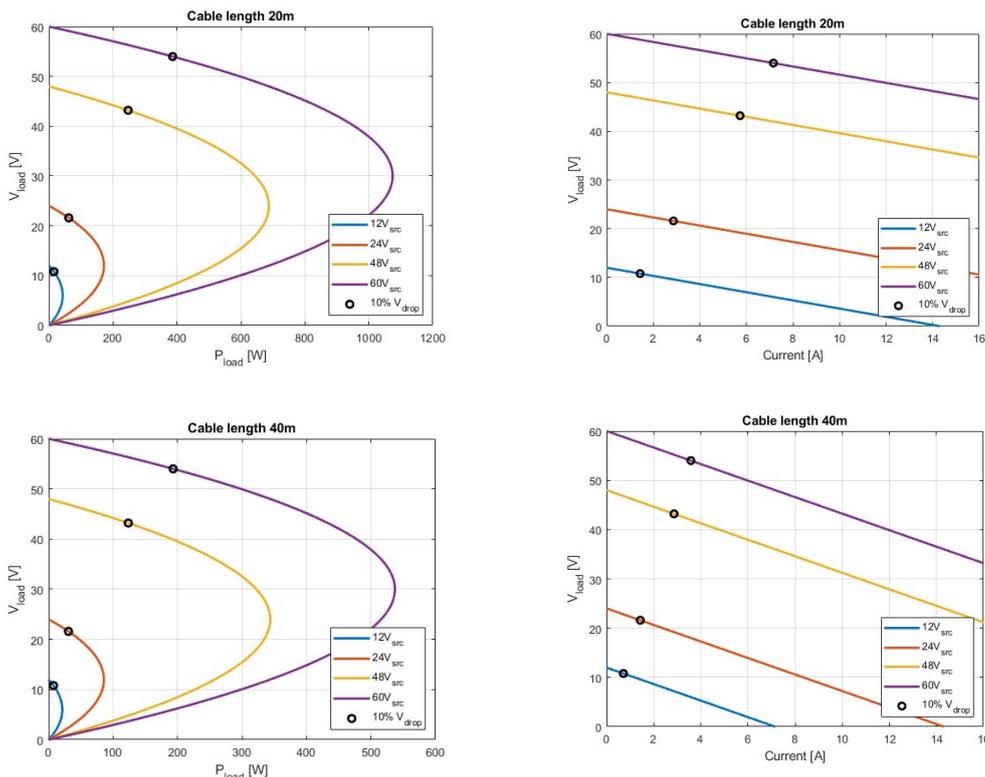


Figure 5: Voltage drop over transmitted power and current for an 18AWG copper wire

On the left side of Figure 5 we can see that if the power increases, the voltage of the load will drop, what is caused by the increase of current through the power pair. Where the voltage drop is 50%, the amount of transferred power is maximal, but typically this maximum is not used due to stability issues it may cause for the PDs.

Most electrical devices accept a minimum voltage of 10% below the rated voltage. Assuming a voltage drop of 10% over the cable, the power efficiency is approximately 80%. This voltage drop is shown by the small black circle. Note that for PoDL the voltage drop can go up to 20%. The results in Figure 5 are shown for cable lengths of 20 and 40m and as expected the cable length has a clear impact on how much power can be transferred. For the maximum length of 40m we can see that with a source voltage of 60V a power close to 200W can be provided and for 20 meters or less up to 400W.

### Galvanic separation

With PoDL the data and power are combined on the same wire pair. Thus, a simple 2-wire cable with a small diameter (also due to the current level below 1.5A) may be used. The downside of this setup is that there are strict requirements regarding noise and rate of change of power levels to avoid disturbances on the data transmission. Typical noise that can be expected on the power lines are voltage ripples coming from switch mode power supplies or from actuators. Therefore, particularly in industrial environments, it is important when implementing PoDL to use good filter circuits to suppress this noise. By separating and even shielding the power from the data pair the interference of the power lines has a much lower impact on the data lines.

To determine the quality of the shielding we need to understand what kind of noise we need to suppress. One type of noise comes from switch mode power supplies that, when properly designed, typically has a voltage ripple between 0.25V and 1V. However, a more disturbing noise can come from actuators like for example DC motors. They can create bursts, which are a repetition of very short pulses in the time domain and create noise over a wide frequency bandwidth. IEC 61000-4-4 describes the test setup for the resilience of electrical systems against such bursts. It defines a pulse like shown in Figure 6 where we also can see the behavior of this burst in the frequency domain. The spectrum of these bursts indicates that it mainly generates noise in the lower MHz range. This means that reducing the impact of the lower frequency noise is the main priority here.

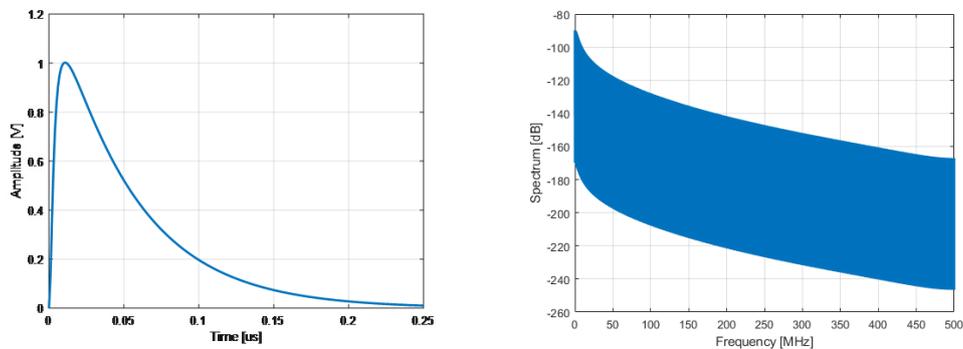


Figure 6: Burst signals as defined in IEC 61000-4-4: (a) Pulse shape in time domain, (b) Spectrum of a burst

To get an idea of the amount of noise an SPE PHY chip can handle, we can follow two IEEE standards as guideline. In IEEE 802.3bu, which describes PoDL, there is the requirement that a maximum ripple voltage of 0.1Vpp is allowed for the frequency range from 1kHz to 10MHz caused by the PSE or PD. From IEEE 802.3bp, which specifies the 1000BASE-T1 media system, we have the requirement for the alien cross-talk noise rejection. Figure 7 shows the associated test circuitry where the noise source provides noise with a Gaussian distribution and a magnitude of -100dBm/Hz to a link segment up to 40m which the PHY chip has to withstand without losing data.

The above-mentioned requirements may be used in simulations and measurements to check the resilience of an SPE link with the hybrid connector and cable against external noise.

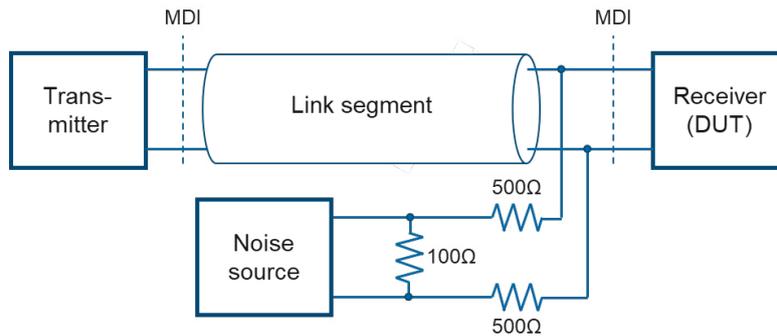


Figure 7: Test setup alien cross-talk noise rejection as defined in IEEE802.3bp

### Power distributions

Another possibility that the separated power and signal contacts bring is the increased flexibility to implement the power distribution in networks. With PoDL designs, only a point-to-point connection is possible. There are investigations ongoing to extend PoDL to power several PDs with one PSE, however those are focused on the 10BASE-T1 media system only. With the additional power line of the hybrid connector more than one PD can be powered as explained below and, of course, PoDL can be used in addition. In case PoDL and separate power are complementarily used, the network for power distribution can be split in a network that can handle noise from all kind of actuators on the separate power lines and in a PoDL network that powers the SPE PHY chips only. Examples of possible topologies to power nodes in a network are shown in Figure 8. Here the power distribution over the separate power lines can be applied point-to-point in case we need to have a lot of power for one PD (8a). It can also be applied over a bus (8b) or over a switch (8c) to power several actuators that can create a high amount of noise. Lastly, when the amount of power is not enough it is always possible to add another PSE (8d).

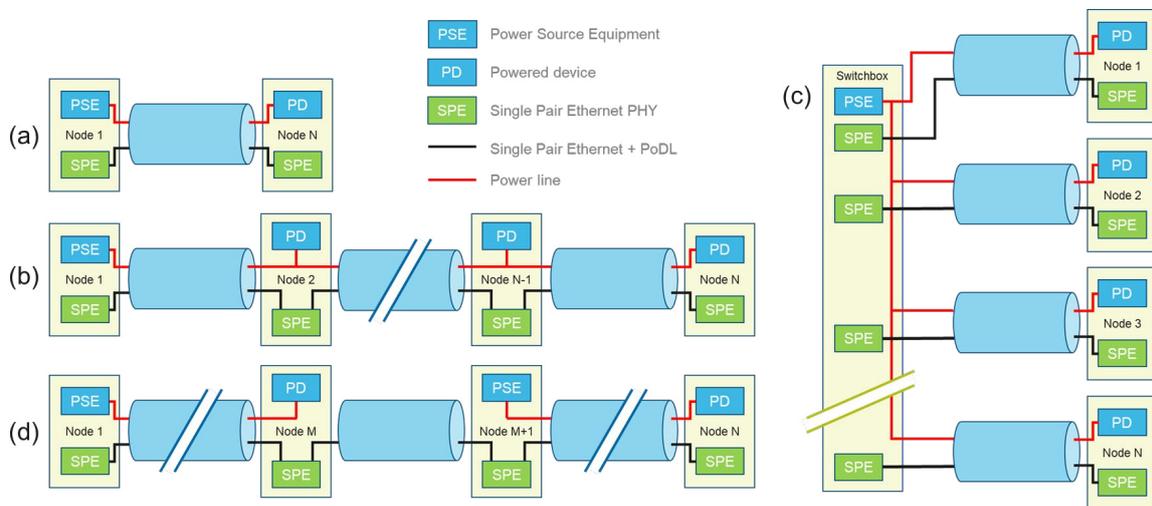


Figure 8: Network topologies hybrid connector: (a) Point to point, (b) Bus powered, (c) Switch possibility, (d) Bus powered with additional resupply points

## Conclusion

A connector has been discussed that is complementary to existing SPE connectors. Next to the SPE interface, that can transfer power by applying PoDL, it contains additional power contacts within a small form factor of an M8 connector. Although the cable attached to the connector gets slightly heavier and wider in diameter, it provides the possibility of higher current levels than possible with PoDL and thus enables higher power delivery. It also provides more flexibility in network topologies. Next to that, it can handle significantly higher EMI disturbances on the power contacts without affecting the data transmission. This makes it an attractive candidate for networks where the actuators and sensors are mounted directly on machines.

## References

- [1] "IEEE802.3bu - IEEE Standard for Ethernet--Amendment 8: Physical Layer and Management Parameters for Power over Data Lines (PoDL) of Single Balanced Twisted-Pair Ethernet," 2016.
- [2] "IEEE 802.3bp - IEEE Standard for Ethernet Amendment 4: Physical Layer Specifications and Management Parameters for 1 Gb/s Operation over a Single Twisted-Pair Copper Cable," 2016.
- [3] "IEC 63171-6: Connectors for electrical and electronic equipment - Part 6: Detail specification for 2-way and 4-way (data/power), shielded, free and fixed connectors for power and data transmission with frequencies up to 600 MHz.," 2020.
- [4] Yair Darshan, "IEEE P802.3bu," September 2014. [Online]. Available: [http://www.ieee802.org/3/bu/public/sep14/darshan\\_3bu\\_1\\_0914.pdf](http://www.ieee802.org/3/bu/public/sep14/darshan_3bu_1_0914.pdf).

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