MAX77540

16V$_{IN}$/6A, Dual-Phase High-Efficiency Buck Converter

General Description

The MAX77540 is a high-efficiency step-down converter with two 3A switching phases. It uses an adaptive COT (constant on-time) current-mode control architecture and the two 3A switching phases can be configured as either one (2Φ, 6A) or two (1Φ, 3A each) outputs. Its wide input voltage range enables a direct conversion for sub-1V outputs from 3-cell Li+ batteries, USB PD, and 12V$_{DC}$ supply rails. The output voltages are preset with resistors and are further adjustable through an I^{2}C-compatible interface. With 94% peak efficiency, low quiescent current, and compact solution size, the MAX77540 is ideal for battery powered, space-constraint equipment.

Programmable switching frequency, frequency tracking, spread-spectrum, and ultrasonic mode allow easier system optimization for noise-sensitive applications. Dedicated EN, POK, and FPWMB pins provide options for direct hardware control, while more programmable options, such as soft-start/stop and ramp-up/down slew-rates, are available through I^{2}C. An array of built-in protections insures safe operation under abnormal operating conditions.

Applications

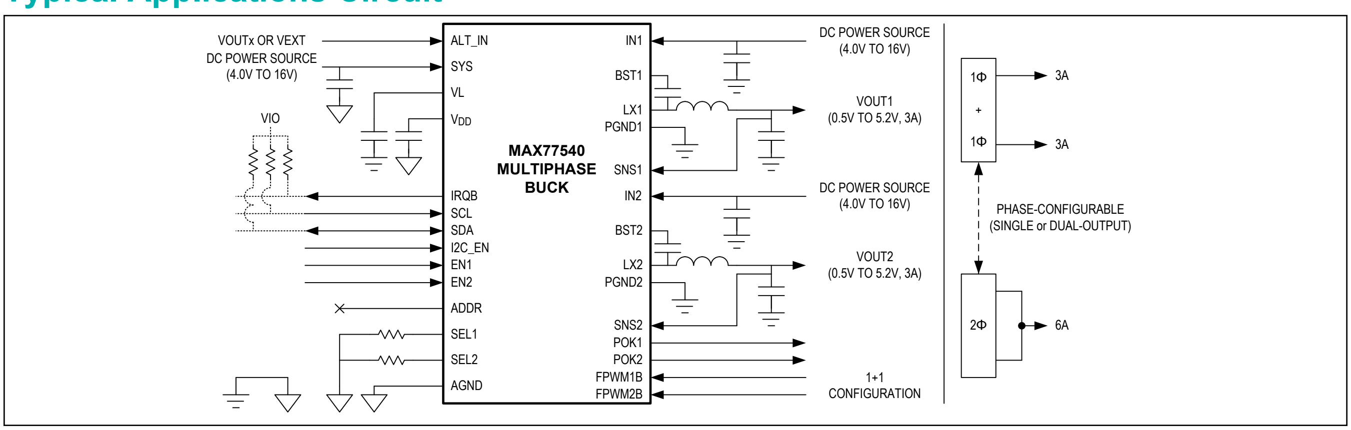
- 2/3-Cell Li+ and USB-C Power Delivery Systems
- Audio and Video Equipment
- Microprocessors, field-programmable gate arrays (FPGAs), digital signal processors (DSPs), and application-specific integrated circuits (ASICs)
- Networking and PCIe®/redundant array of inexpensive disks (RAID) Cards

Benefits and Features

- 4V to 16V Input Voltage Range
- 0.5V to 5.2V Output Voltage Range
- Resistor Configurable Default V$_{OUT}$
- Two 3A Bucks (1Φ) or One 6A Buck (2Φ)
- ±0.5% V$_{OUT}$ Accuracy (Default V$_{OUT}$ at 25°C)
- 94% Peak Efficiency (7.6V$_{IN}$, 3.3V$_{OUT}$, 1MHz)
- Auto SKIP/PWM and Low-Power Mode
- 98% Max. Duty Cycle Dropout Operation
- Programmable Soft-Start/Stop and Ramp-Up/Down Slew Rates
- Pre-Biased Startup and Active Output Discharge
- Programmable Inductor Peak Current Limits
- 0.5/1.0/1.6MHz Nominal Switching Frequency
- Spread-Spectrum Modulation
- Internal/External Frequency Tracking
- Ultrasonic Mode
- Dedicated EN, POK, and FPWM Pins
- Undervoltage lockout (UVLO), Thermal Shutdown, and Short-Circuit Protection
- High-Speed I^{2}C I/F with 3-Slave Address Options
- 30-WLP (2.51mm x 2.31mm) and 24-FC2QFN (3mm x 3mm) Packages
- Less than 55mm^2 Total Solution Size

***Ordering Information** appears at end of data sheet.*

Typical Applications Circuit



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Absolute Maximum Ratings

SYS to AGND ... -0.3V to +17.6V
ALT_IN to AGND ... -0.3V to +6.0V
V_{DD} to AGND ... -0.3V to +2.2V
V_L to PGND ... -0.3V to +2.2V
I2C_EN to AGND ... -0.3V to MIN(V_{SYS} + 0.3, +17.6)V
EN1, EN2 to AGND ... -0.3V to MIN(V_{SYS} + 0.3, +17.6)V
IN1 to PGND1 ... -0.3V to +17.6V
IN2 to PGND2 ... -0.3V to +17.6V
BSTx to LXx ... -0.3V to +2.2V
SNS1, SNS2 to AGND ... -0.3V to +6.0V
FPWM1B, FPWM2B to AGND ... -0.3V to +6.0V
POK1, POK2 to AGND ... -0.3V to +6.0V
SCL, SDA, IRQB to AGND ... -0.3V to +6.0V
ADDR, SEL1, SEL2 to AGND ... -0.3V to MIN(V_{DD} + 0.3, +2.2)V
PGND1, PGND2 to AGND ... -0.3V to +0.3V
Continuous Power Dissipation (JESD51-7, T_A = +70ºC)
  30 WLP (Derate 20.25mW/°C above +70°C) ... 1620mW
Junction Temperature ... +150°C
Storage Temperature Range ... -65°C to +150°C
Soldering Temperature (reflow) ... +260°C

Note 1: LXx has internal clamp diodes to its corresponding PGNDx and INx. Applications that forward bias these diodes should take care not to exceed the IC's package power dissipation limits.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

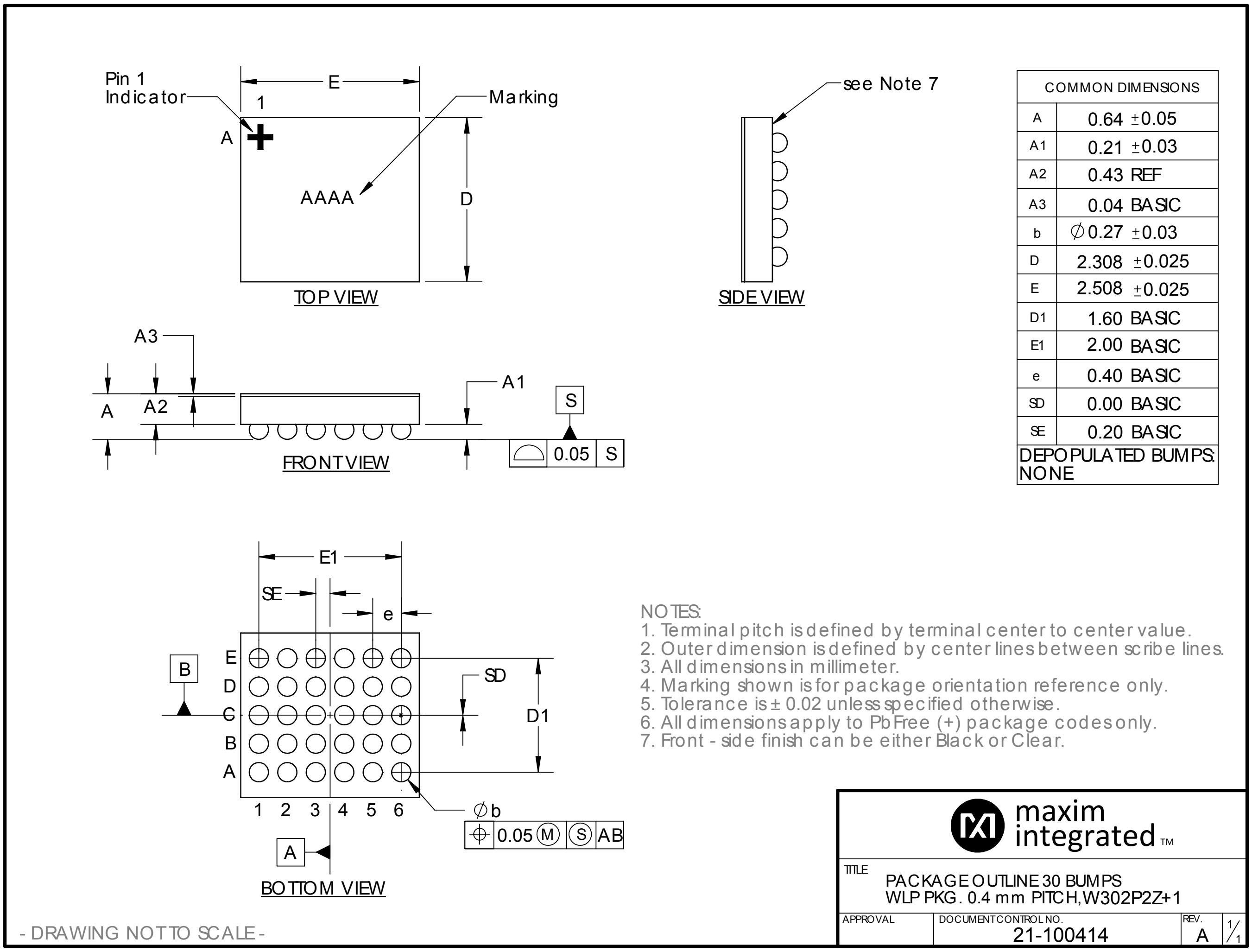
PARAMETER	SYMBOL	CONDITION	TYPICAL RANGE	UNIT
Input Voltage Range	V_{IN}		4 to 16	V
Output Current Range	I_{OUT}	For continuous operation at 3A, the junction temperature (T_J) is limited to +105ºC. If the junction temperature is higher than +105ºC, the expected lifetime at 3A continuous operation is derated.	0 to 3	A
Junction Temperature Range	T_J		-40 to +125	ºC

Note: These limits are not guaranteed.

Package Information

30 WLP

Package Code	W302P2Z+1
Outline Number	21-100414
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient ($θ_{JA}$)	49.38°C/W



For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics—Top-Level

(V_{SYS} = V_{IN1} = V_{IN2} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 5.0V, Single-phase Configuration (1Φ + 1Φ), V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT VOLTAGE AND SUPPLY CURRENT						
SYS Voltage Range	V_{SYS}		4		16	V
SYS Undervoltage Lockout (UVLO)	V_{UVLO_R}	V_{SYS} rising	3.8	3.9	4.0	V
	V_{UVLO_F}	V_{SYS} falling	3.5	3.7	3.8	
Power-On Reset (POR) Threshold (Note 7)	V_{POR}	V_{SYS} falling		1.7		V

Electrical Characteristics—Top-Level (continued)

(V_{SYS} = V_{IN1} = V_{IN2} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 5.0V, Single-phase Configuration (1Φ + 1Φ), V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown Supply Current (Note 3)	I_{SHDN}	V_{I2C_EN} = V_{ENx} = 0V	T_A = -40°C to +85°C		1.5	5.5	µA
			T_A = +125°C			15	
Standby Supply Current (Note 3)	I_{STBY}	V_{ALT_IN} = 0V, EN_FTMON = 0, all Bucks are disabled	T_A = -40°C to +85°C		25	50	µA
			T_A = +125°C			70	
Quiescent Supply Current with External ALT_IN (Note 3)	I_Q	V_{ALT_IN} = V_{EXT} = 3.3V, V_{OUT} > $V_{OUT(TARGET)}$, both Buck phases are enabled, SKIP or LP-SKIP mode, no load			10	20	µA
Quiescent Supply Current in LP-SKIP Mode (Note 3)	$I_{Q\_LP-SKIP}$	V_{ALT_IN} = 0V, V_{OUT} > $V_{OUT(TARGET)}$, no load	Only one Buck phase is enabled		215	300	µA
			Both Buck phases are enabled		310	400	
Quiescent Supply Current in SKIP Mode (Note 3)	I_{Q_SKIP}	V_{ALT_IN} = 0V, V_{OUT} > $V_{OUT(TARGET)}$, no load	Only one Buck phase is enabled		260	350	µA
			Both Buck phases are enabled		400	500	
INTERNAL BIAS SUPPLY							
V_L Regulator Voltage	V_L	(Note 4)			1.8		V
V_{DD} Regulator Voltage	V_{DD}	(Note 4)			1.8		V
V_{DD} Undervoltage Lockout (UVLO)	$V_{DD\_UVLO\_F}$	(Note 4)			1.55		V
ALT_IN Switch-Over Threshold	V_{SWO}	V_{ALT_IN} Rising, 100mV hysteresis, V_L & V_{DD} input switches from SYS to ALT_IN above this threshold (WLP package only)		2.7	2.8	2.9	V
ALT_IN Valid Voltage Range	V_{ALT_IN}			V_{SWO}		5.5	V
ALT_IN Shutdown Supply Current	$I_{SHDN\_ALT\_IN}$	V_{I2C_EN} = V_{ENx} = 0V, V_{ALT_IN} = 3.3V			0.2		µA
THERMAL PROTECTION							
Thermal Warning 1	T_{J120}	T_J rising, 15°C hysteresis			+120		°C
Thermal Warning 2	T_{J140}	T_J rising, 15°C hysteresis			+140		°C
Thermal Shutdown (T_{SHDN})	T_{SHDN}	T_J rising, 15°C hysteresis			+165		°C
LOGIC INPUT AND OUTPUT							
ADDR Input Logic High Threshold	V_{IH_ADDR}			0.8 x V_{DD}			V
ADDR Input Logic Low Threshold	V_{IL_ADDR}					0.2 x V_{DD}	V
FPWMxB Input Logic High Threshold	V_{IH_FPWMxB}			1.44			V

Electrical Characteristics—Top-Level (continued)

(V_{SYS} = V_{IN1} = V_{IN2} = 12V, V_{OUT1} = 3.3V, V_{OUT2} = 5.0V, Single-phase Configuration (1Φ + 1Φ), V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FPWMxB Input Logic Low Threshold	V_{IL_FPWMxB}					0.54	V
I2C_EN, ENx Input Logic High Threshold	V_{IH_EN}			1.1			V
I2C_EN, ENx Input Logic Low Threshold	V_{IL_EN}					0.4	V
IRQB Output Logic Low Threshold	V_{OL_IRQB}	Sinking 2mA				0.4	V
POKx Output Logic Low Threshold	V_{OL_POK}	Sinking 2mA				0.4	V
ADDR Leakage Current	I_{LKG_ADDR}	V_{DD} = 1.8V, V_{ADDR} = 0V and 1.8V	T_A = +25°C	-1	±0.001	+1	µA
			T_A = +85°C		±0.01		
I2C_EN, ENx Leakage Current	I_{LKG_EN}	V_{SYS} = 16V, V_{ENx} = 0V and 16V	T_A = +25°C		±0.1		µA
			T_A = +85°C		±0.5		
IRQB Leakage Current	I_{LKG_IRQB}	IRQB set to Hi-Z (i.e., No Interrupt Pending), V_{IRQB} = 0V and 5.5V		-1		+1	µA
POKx Leakage Current	I_{LKG_POK}	POKx = High (Hi-Z), V_{POKx} = 5.5V, T_A = +85ºC				1	µA

Electrical Characteristics—Dual-Phase Configurable Buck Converter

(V_{SYS} = V_{IN1} = V_{IN2} = 12V, Single-phase Configuration (1Φ+1Φ), V_{OUT1} = 3.3V, V_{OUT2} = 5.0V, V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage Range	V_{INx}		4		16	V
DC OUTPUT VOLTAGE AND ACCURACY						
Output Voltage Range	V_{OUT_RNG}	Low-range (Mx_RNG[1:0] = 0x0)	0.5		1.2	V
		Mid-range (Mx_RNG[1:0] = 0x1)	1		2.4	
		High-range (Mx_RNG[1:0] = 0x2)	2		5.2	
Line Regulation		1Φ, FPWM Mode, V_{INx} = 4V to 16V, V_{OUT} = Default, I_{OUT} = 0A	-0.1		+0.1	%/V
Load Regulation		1Φ, FPWM Mode, I_{OUT} = 0A to 3A (Note 7)		0.1		%/A

Electrical Characteristics—Dual-Phase Configurable Buck Converter (continued)

(V_{SYS} = V_{IN1} = V_{IN2} = 12V, Single-phase Configuration (1Φ+1Φ), V_{OUT1} = 3.3V, V_{OUT2} = 5.0V, V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC Output Voltage Accuracy	V_{OUT_ACC}	1Φ, FPWM Mode, V_{INx} = 4V to 16V, I_{OUT} = 0A	V_{OUT} < 0.6V	-2.5		+2.5	%
			0.6V ≤ V_{OUT} < 4.0V	-1.5		+1.5	
			4.0V ≤ V_{OUT} ≤ 5.2V	-1.0		+1.0	
			V_{OUT} = Factory Default, T_A = +25°C	-0.5		+0.5	
POWER STAGE							
High-Side MOSFET Peak Current Limit	I_{PLIM}	Mx_ILIM[1:0] = 0x0		1.10	1.50	1.90	A
		Mx_ILIM[1:0] = 0x1		1.85	2.25	2.65	
		Mx_ILIM[1:0] = 0x2		2.55	3.00	3.45	
		Mx_ILIM[1:0] = 0x3		4.05	4.50	4.95	
Low-Side MOSFET Valley Current Limit	I_{VLIM}	Tracks I_{PLIM}			I_{PLIM} - 1A		A
Low-Side MOSFET Negative Current Limit	I_{NLIM}	FPWM Mode		-3.6	-2.9	-2.2	A
Low-Side MOSFET Zero-Crossing Current Threshold	I_{ZX}	SKIP or LP-SKIP Mode			150		mA
High-Side MOSFET On-Resistance	R_{ON_HS}	1Φ, I_{LXx} = 190mA			50	100	mΩ
Low-Side MOSFET On-Resistance	R_{ON_LS}	1Φ, I_{LXx} = -190mA			32	64	mΩ
Nominal Switching Frequency	F_{SW}	FPWM Mode, No Load, No External Clock, T_A = +25°C (Note 5)	Mx_FREQ[1:0] = 0x0		0.5		MHz
			Mx_FREQ[1:0] = 0x1		1		
			Mx_FREQ[1:0] = 0x2 or 0x3		1.6		
Minimum Switching Frequency	$F_{SW(MIN)}$	Mx_ULTRA = 0	LP-SKIP Mode	7.0	7.8	8.6	kHz
			SKIP or DROPOUT Mode	14.0	15.6	17.2	
		Mx_ULTRA = 1	LP-SKIP, SKIP, or DROPOUT Mode	90	100	110	
Maximum Duty Cycle	D_{MAX}	Dropout Region (V_{OUT} falls below its regulation target)		97	98		%

Electrical Characteristics—Dual-Phase Configurable Buck Converter (continued)

(V_{SYS} = V_{IN1} = V_{IN2} = 12V, Single-phase Configuration (1Φ+1Φ), V_{OUT1} = 3.3V, V_{OUT2} = 5.0V, V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LX Active Discharge Resistance	R_{AD1}	1Φ, Buck Output disabled, Active Discharge enabled (Mx_ADIS1 = 1), Resistance from corresponding LX_X to PGNDx		1		Ω
	R_{AD100}	1Φ, Buck Output disabled, Active Discharge enabled (Mx_ADIS100 = 1), Resistance from corresponding LX_X to PGNDx		100		
LX Leakage Current	I_{LKG_LX}	1Φ, V_{LXx} = 0V and 16V, T_A = +25°C		0.6	4.5	μA
		1Φ, V_{LXx} = 0V and 16V, T_A = -40°C to +85°C		1		
SLEW RATE AND TIMING						
Soft-Start Slew Rate (Note 6)	$\Delta V_{OUT}/\Delta t$	SSTRT_SR[2:0] = 0x0		0.15		mV/μs
		SSTRT_SR[2:0] = 0x1		0.625		
		SSTRT_SR[2:0] = 0x2		1.25		
		SSTRT_SR[2:0] = 0x3		2.5		
		SSTRT_SR[2:0] = 0x4		5		
		SSTRT_SR[2:0] = 0x5		10		
		SSTRT_SR[2:0] = 0x6		20		
		SSTRT_SR[2:0] = 0x7		40		
Soft-Stop Slew Rate (Note 6)	$\Delta V_{OUT}/\Delta t$	SSTOP_SR[2:0] = 0x0		-0.15		mV/μs
		SSTOP_SR[2:0] = 0x1		-0.625		
		SSTOP_SR[2:0] = 0x2		-1.25		
		SSTOP_SR[2:0] = 0x3		-2.5		
		SSTOP_SR[2:0] = 0x4		-5		
		SSTOP_SR[2:0] = 0x5		-10		
		SSTOP_SR[2:0] = 0x6		-20		
		SSTOP_SR[2:0] = 0x7		-40		
Ramp-Up Slew Rate (Note 6)	$\Delta V_{OUT}/\Delta t$	Mx_RU_SR[2:0] = 0x0		0.15		mV/μs
		Mx_RU_SR[2:0] = 0x1		0.625		
		Mx_RU_SR[2:0] = 0x2		1.25		
		Mx_RU_SR[2:0] = 0x3		2.5		
		Mx_RU_SR[2:0] = 0x4		5		
		Mx_RU_SR[2:0] = 0x5		10		
		Mx_RU_SR[2:0] = 0x6		20		
		Mx_RU_SR[2:0] = 0x7		40		

Electrical Characteristics—Dual-Phase Configurable Buck Converter (continued)

(V_{SYS} = V_{IN1} = V_{IN2} = 12V, Single-phase Configuration (1Φ+1Φ), V_{OUT1} = 3.3V, V_{OUT2} = 5.0V, V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Ramp-Down Slew Rate (Note 6)	$\Delta V_{OUT}/\Delta t$	Mx_RD_SR[2:0] = 0x0			-0.15		mV/µs
		Mx_RD_SR[2:0] = 0x1			-0.625		
		Mx_RD_SR[2:0] = 0x2			-1.25		
		Mx_RD_SR[2:0] = 0x3			-2.5		
		Mx_RD_SR[2:0] = 0x4			-5		
		Mx_RD_SR[2:0] = 0x5			-10		
		Mx_RD_SR[2:0] = 0x6			-20		
		Mx_RD_SR[2:0] = 0x7			-40		
Slew-Rate Accuracy		REFDAC slew-rate accuracy		-5		+5	%
Turn-On Delay	t_{DLY}	Delay from rising edge of ENx signal to V_{OUTx} ramping start-off	V_L is pre-enabled (I2C_EN = high)		100	140	µs
			V_L is not pre-enabled (I2C_EN = low)		435	535	
FREQUENCY TRACKING							
External Frequency Tracking Lockable Range (Note 6)	F_{FTRAK}	Expressed as a percentage of the nominal frequency set by Mx_FREQ[1:0]		95		105	%
SPREAD-SPECTRUM							
Modulation Frequency (Note 6)	F_{SS_MOD}	Mx_SS_FREQ[1:0] = 0x0			1		kHz
		Mx_SS_FREQ[1:0] = 0x1			3		
		Mx_SS_FREQ[1:0] = 0x2			5		
		Mx_SS_FREQ[1:0] = 0x3			7		
Modulation Envelope	ΔF_{SS}	Mx_SS_ENV[1:0] = 0x1			±8		%
		Mx_SS_ENV[1:0] = 0x2			±12		
		Mx_SS_ENV[1:0] = 0x3			±16		
POWER-OK AND SHORT-CIRCUIT PROTECTION							
Power-OK Rising Threshold	V_{POK_R}	Expressed as a percentage of V_{OUT}		77	82	87	%
Power-OK Falling Threshold	V_{POK_F}	Expressed as a percentage of V_{OUT}		73	78	83	%
Short-Circuit Detection Threshold	V_{SCP}	V_{OUT} Falling, Expressed as a percentage of target V_{OUT}			20		%
Power-OK Fault Timeout (Note 6)	t_{POK_TO}	POK_TO[1:0] = 0x1			25		ms
		POK_TO[1:0] = 0x2			50		
		POK_TO[1:0] = 0x3			100		

Electrical Characteristics—I^2C Serial Interface

(V_{SYS} = 12V, V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O STAGE						
SCL, SDA Input Logic Low Threshold	V_{IL}				0.54	V
SCL, SDA Input Logic High Threshold	V_{IH}		1.44			V
SCL, SDA Input Hysteresis	V_{HYS}			0.3		V
SDA Output Logic Low Threshold	V_{OL_SDA}	Sinking 20mA			0.4	V
SCL, SDA Input Leakage Current	I_{LKG}	V_{SCL} = V_{SDA} = 0V or 5.5V	-10		+10	µA
SCL, SDA Pin Capacitance		(Note 7)		10		pF
TIMING (STANDARD, FAST, AND FAST-MODE PLUS)						
Clock Frequency	f_{SCL}				1	MHz
Hold Time (REPEATED) START Condition	$t_{HD;STA}$		260			ns
SCL LOW Period	t_{LOW}		500			ns
SCL HIGH Period	t_{HIGH}		260			ns
Setup Time REPEATED START Condition	$t_{SU;STA}$		260			ns
Data Hold Time	$t_{HD;DAT}$		0			µs
Data Setup Time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		260			ns
Bus Free Time between STOP and START Condition	t_{BUF}		0.5			µs
Input Filter Suppressed Spike Pulse Width	t_{SP}	(Note 7)		50		ns
TIMING (HIGH-SPEED MODE)						
Clock Frequency	f_{SCL}	High-speed mode			3.4	MHz
Setup Time REPEATED START Condition	$t_{SU;STA}$		160			ns
Hold Time (REPEATED) START Condition	$t_{HD;STA}$		160			ns
SCL LOW Period	t_{LOW}		160			ns
SCL HIGH Period	t_{HIGH}		60			ns
Data Setup Time	$t_{SU;DAT}$		10			ns
Data Hold Time	$t_{HD;DAT}$		0			µs
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns

Electrical Characteristics—I^{2}C Serial Interface (continued)

(V_{SYS} = 12V, V_{I2C_EN} = 1.8V, T_A = T_J = -40°C to +125°C, typical values are at T_A = T_J = +25°C, unless otherwise noted. Note 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Filter Suppressed Spike Pulse Width	t_{SP}	(Note 7)		10		ns

Note 2: The MAX77540 is tested under pulsed load conditions such that $T_J \approx T_A$. Limits over the operating temperature range (T_J = -40°C to +125°C) are guaranteed by design and characterization using statistical process control methods. Note that the maximum ambient temperature consistent with this specification is determined by specific operating conditions, board layout, rated package thermal impedance, and other environmental factors.

Note 3: Supply Current = $I_{SYS} + I_{IN1} + I_{IN2}$

Note 4: See the *Dedicated Internal Supplies* section.

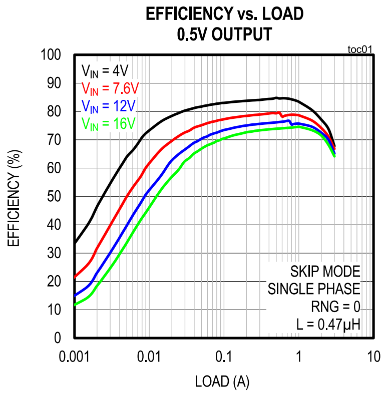
Note 5: Switching frequency is not set by a clock oscillator. F_{SW} varies depending on input voltage, output voltage, load, and spread-spectrum settings.

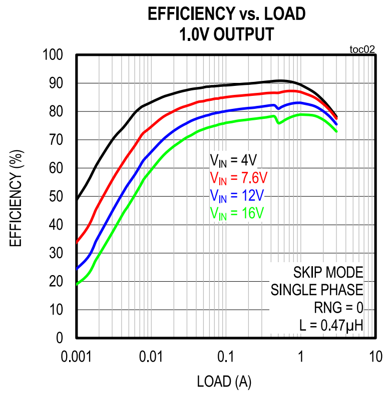
Note 6: Guaranteed by design. Production tested through scan.

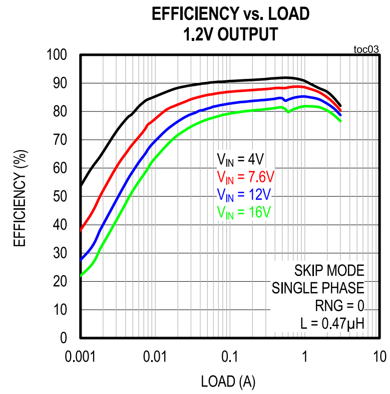
Note 7: Not production tested. Design guidance only.

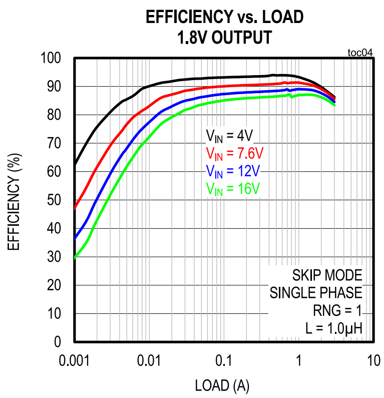
Typical Operating Characteristics

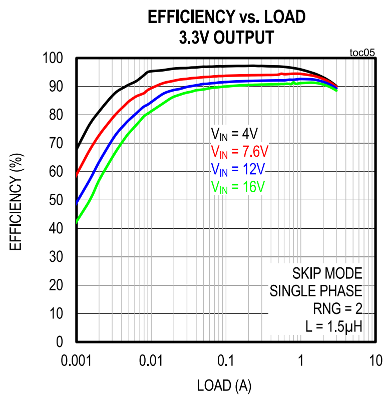
(V_{IN} = 12V, V_{OUT} = 3.3V, L = 1μH (Murata DFE2520F-1R0M), Skip Mode, Single Phase, F_{SW} = 1MHz, T_A = +25°C, unless otherwise noted.)

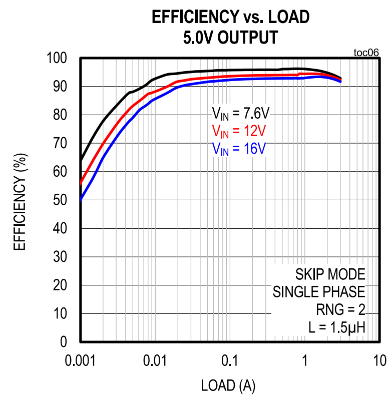


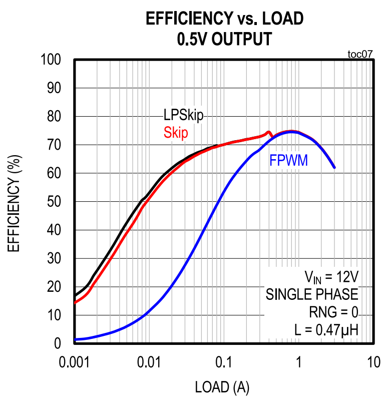


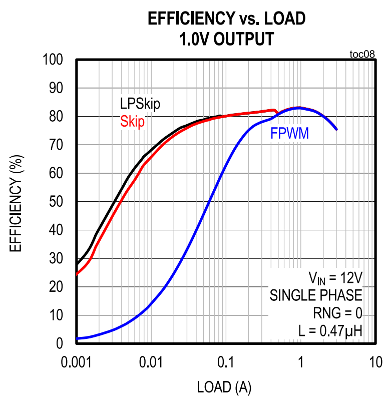


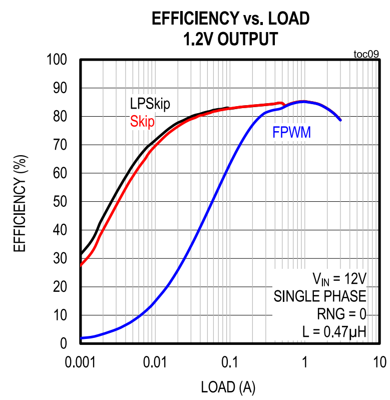






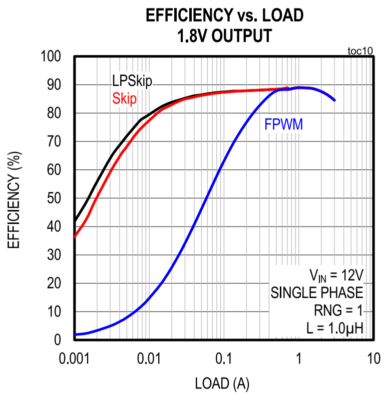


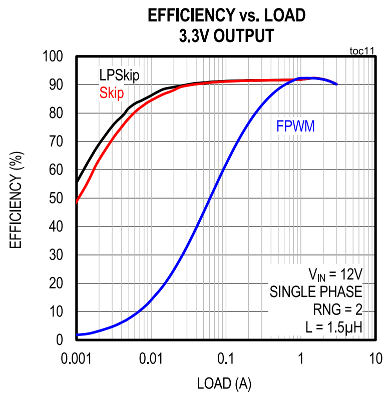


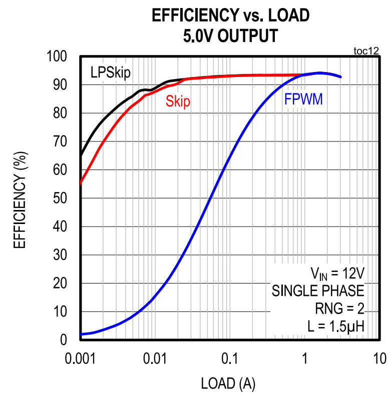


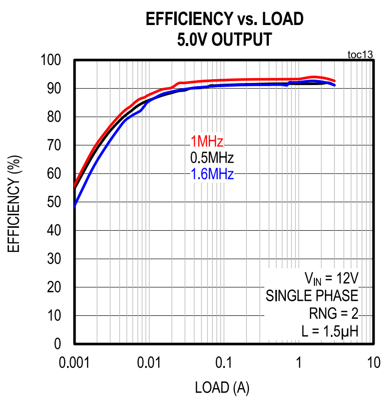
Typical Operating Characteristics (continued)

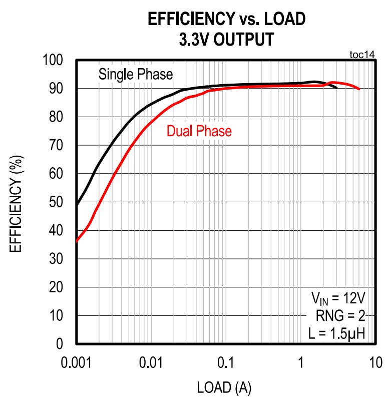
(V_{IN} = 12V, V_{OUT} = 3.3V, L = 1μH (Murata DFE2520F-1R0M), Skip Mode, Single Phase, F_{SW} = 1MHz, T_A = +25°C, unless otherwise noted.)

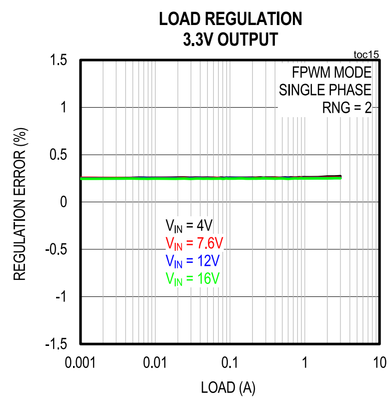


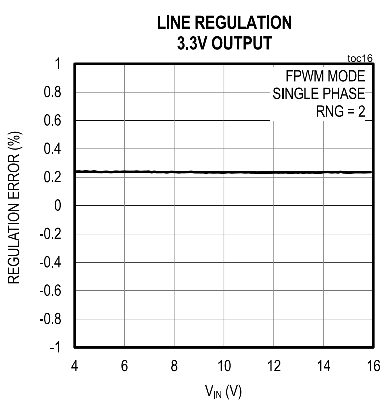


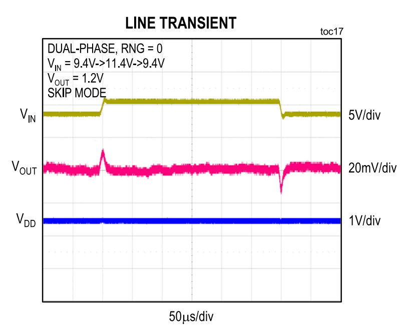


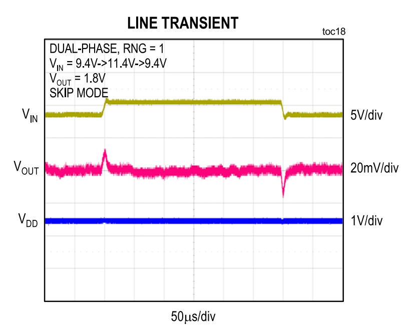






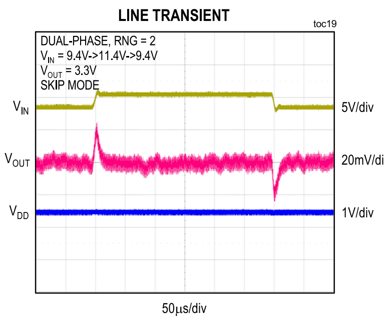


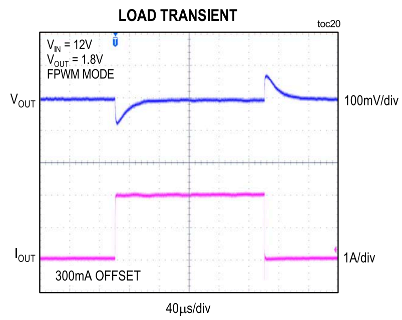


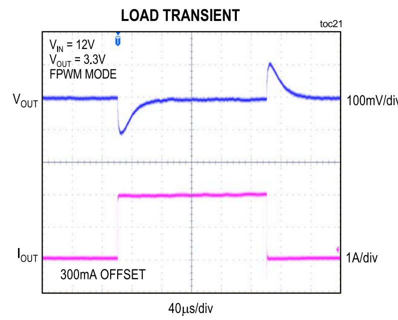


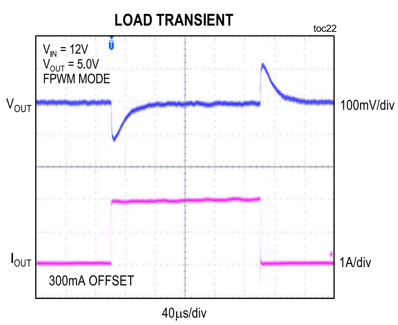
Typical Operating Characteristics (continued)

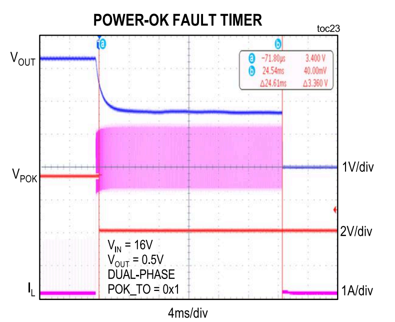
(V_{IN} = 12V, V_{OUT} = 3.3V, L = 1µH (Murata DFE2520F-1R0M), Skip Mode, Single Phase, F_{SW} = 1MHz, T_A = +25°C, unless otherwise noted.)

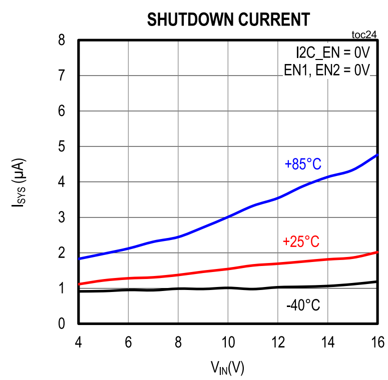


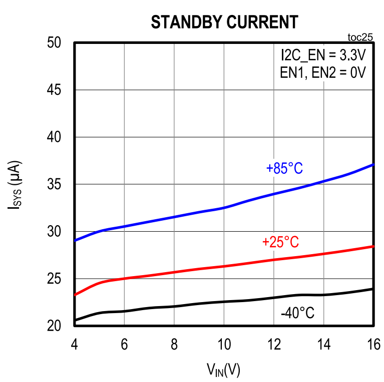


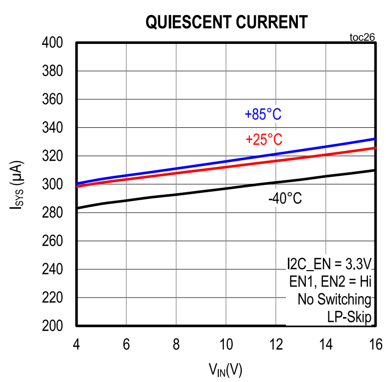


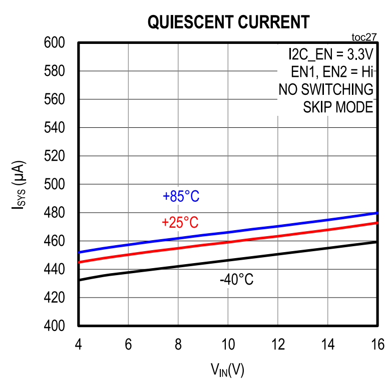








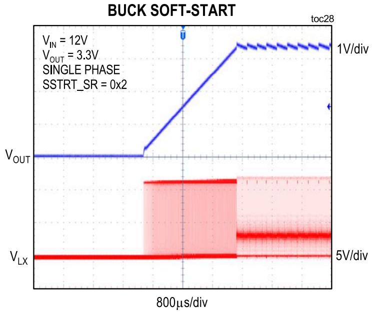




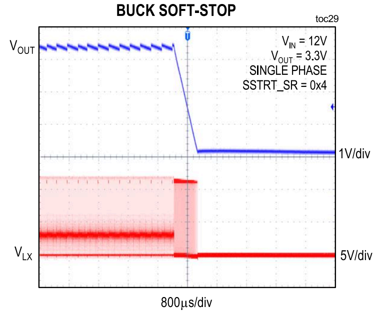
Typical Operating Characteristics (continued)

(V_{IN} = 12V, V_{OUT} = 3.3V, L = 1µH (Murata DFE2520F-1R0M), Skip Mode, Single Phase, F_{SW} = 1MHz, T_A = +25°C, unless otherwise noted.)

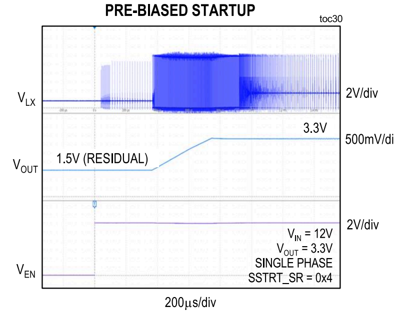
BUCK SOFT-START



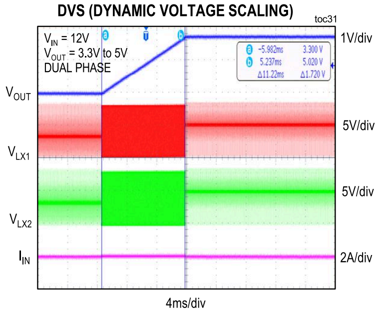
BUCK SOFT-STOP



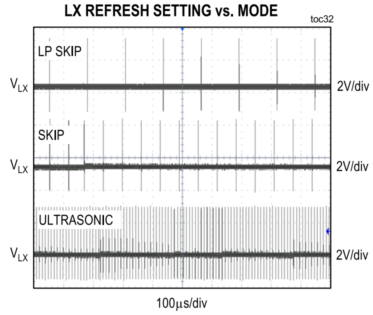
PRE-BIASED STARTUP



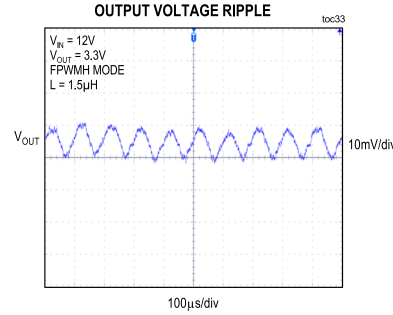
DVS (DYNAMIC VOLTAGE SCALING)



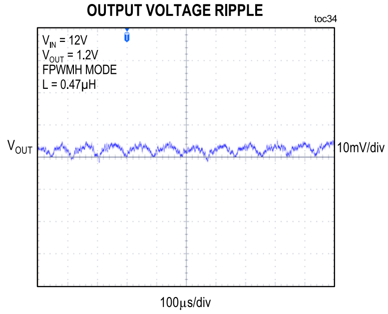
LX REFRESH SETTING vs. MODE



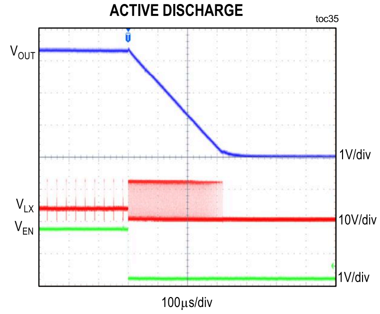
OUTPUT VOLTAGE RIPPLE



OUTPUT VOLTAGE RIPPLE

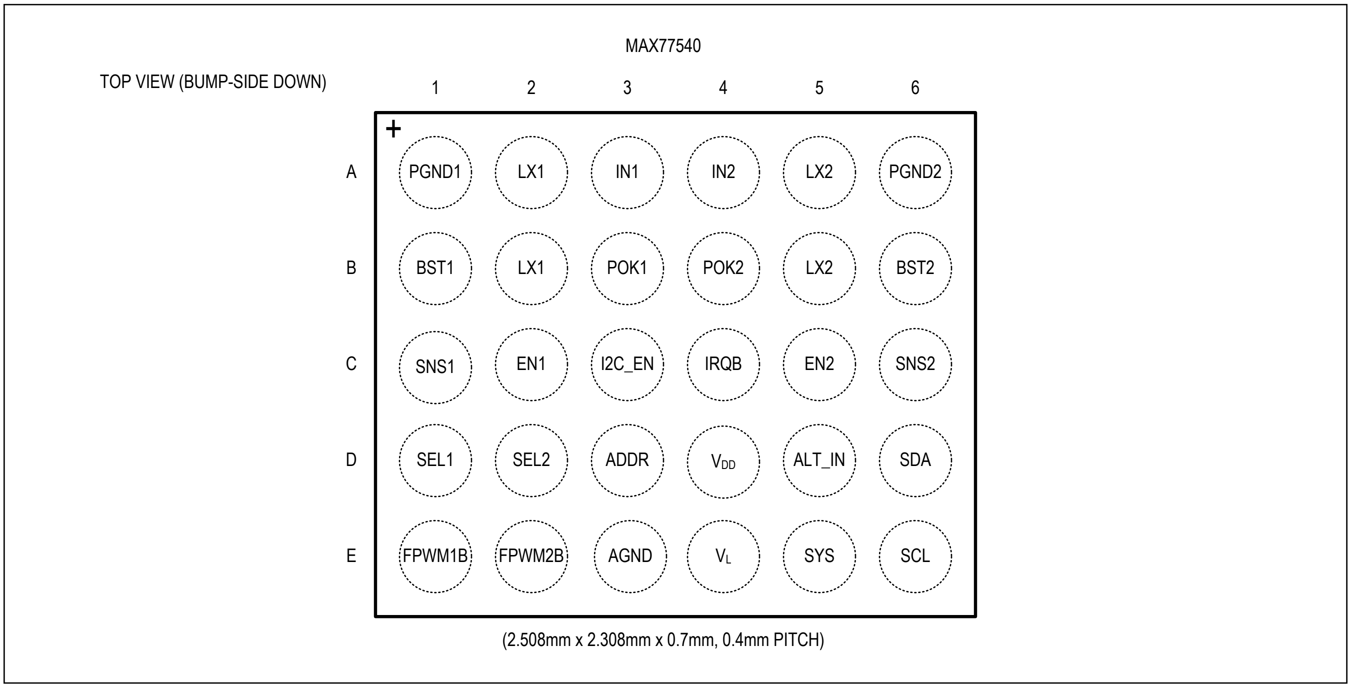


ACTIVE DISCHARGE



Bump Configuration

30 WLP



Bump Descriptions

PIN	NAME	FUNCTION	TYPE
BUCK SWITCHING PHASE			
B1	BST1	Phase1 High-Side MOSFET Driver Supply. Connect a 0.1μF ceramic capacitor between BST1 and LX1.	Power Input
B6	BST2	Phase2 High-Side MOSFET Driver Supply. Connect a 0.1μF ceramic capacitor between BST2 and LX2.	Power Input
A3	IN1	Phase1 Input. Bypass to PGND1 with a 10μF ceramic capacitor.	Power Input
A4	IN2	Phase2 Input. Bypass to PGND2 with a 10μF ceramic capacitor.	Power Input
A2, B2	LX1	Phase1 Switching Node	Power Output
A5, B5	LX2	Phase2 Switching Node	Power Output
A1	PGND1	Phase1 Power Ground	Power Ground
A6	PGND2	Phase2 Power Ground	Power Ground
C1	SNS1	Phase1 Output Voltage Sensing Input. Connect to the output at the point-of-load.	Analog Input
C6	SNS2	Phase2 Output Voltage Sensing Input. Connect to the output at the point-of-load. Connect to AGND or leave unconnected (floating) when the phase configuration is set for 2Φ operation.	Analog Input
INTERNAL BIAS SUPPLY			
E3	AGND	Analog (Quiet) Ground	Ground

Bump Descriptions (continued)

PIN	NAME	FUNCTION	TYPE
D5	ALT_IN	Alternative Power Input for V_L and V_{DD}. Bypass to AGND with a 2.2µF ceramic capacitor when used. See the *Alternative Low-Voltage Input (ALT_IN)* section for more information.	Power Input
E5	SYS	System Power Input (Supply to Internal V_L and V_{DD} Linear Regulator). Bypass to AGND with a 2.2µF ceramic capacitor.	Power Input
D4	V_{DD}	Internal Bias Supply Output. Powered from SYS or ALT_IN depending on V_{ALT_IN}. See the *Alternative Low-Voltage Input (ALT_IN)* section for more information. Bypass to AGND with a 1µF ceramic capacitor. Do not load this pin externally.	Power Output
E4	V_L	Internal Gate Driver Supply Output. Powered from SYS or ALT_IN depending on V_{ALT_IN}. See the *Alternative Low-Voltage Input (ALT_IN)* section for more information. Bypass V_L to PGND with a 2.2µF ceramic capacitor. Do not load this pin externally.	Power Output
CONTROL AND SERIAL INTERFACE			
D3	ADDR	I^2C Slave Address Selection Input (Tri-State). Connect to V_{DD}, ground, or leave unconnected to set I^2C slave address. See the *Slave Address* section for more information.	Digital Input
C2	EN1	Buck1 Enable Input (Active-High). V_{EN1} must not be higher than V_{SYS}.	Digital Input
C5	EN2	Buck2 Enable Input (Active-High). V_{EN2} must not be higher than V_{SYS}. This pin is a 'don't care' when the phase configuration is set for 2Φ operation.	Digital Input
E1	FPWM1B	Buck1 Forced-PWM Mode Control (Active-Low) and External Frequency Tracking Input. Provide an external clock to enable FPWM mode with external frequency stabilization. Connect to V_L if unused. See the *Frequency Tracking (FTRAK)* section for more information.	Digital Input
E2	FPWM2B	Buck2 Forced-PWM Mode Control (Active-Low) and External Frequency Tracking Input. Provide an external clock to enable FPWM mode with external frequency stabilization. Connect to V_L if unused. See the *Frequency Tracking (FTRAK)* section for more information. This input is a 'don't care' when the phase configuration is set for 2Φ operation.	Digital Input
C3	I2C_EN	I^2C Enable Input (Active-High). Enables I^2C interface and V_L & V_{DD} regulators. V_{I2C_EN} must not be higher than V_{SYS}. See the *Dedicated Internal Supplies* section for more information.	Digital Input
C4	IRQB	Interrupt Output (Open-Drain, Active-Low), This pin requires an external pullup resistor. Leave this pin unconnected if unused.	Digital Output
B3	POK1	Buck1 Power-OK Output (Open-Drain). An external pullup resistor (10kΩ to 100kΩ) is required. Leave this pin unconnected if unused.	Digital Output
B4	POK2	Buck2 Power-OK Output (Open-Drain). An external pullup resistor (10kΩ to 100kΩ) is required. Leave this pin unconnected if unused. This pin is pulled low internally when the phase configuration is set for 2Φ operation.	Digital Output
E6	SCL	I^2C Serial Interface Clock. Connect to ground if not used.	Digital Input
D6	SDA	I^2C Serial Interface Data. Connect to ground if not used.	Digital I/O
D1	SEL1	Buck1 Default V_{OUT} Selection Input. Connect a selection resistor (R_{SEL1}) between SEL1 and AGND to configure the default V_{OUT}, V_{OUT} range, and switching frequency for Buck1. Default settings can be overwritten through I^2C. See the *Default Output Voltage Selection (SELx)* section for more information.	Analog Input

Bump Descriptions (continued)

PIN	NAME	FUNCTION	TYPE
D2	SEL2	Buck2 Default V_{OUT} Selection Input. Connect a selection resistor (R_{SEL2}) between SEL2 and AGND to configure the default target V_{OUT}, V_{OUT} range, and switching frequency, and range for Buck2. Default settings can be overwritten through I^2C. When $R_{SEL2} \leq 95.3\Omega$, Buck2 becomes a slave phase of a dual-phase converter. See the *Default Output Voltage Selection (SELx)* section for more information.	Analog Input

Detailed Description—Top-Level

Dedicated Internal Supplies

The MAX77540 has dedicated internal supplies which are the V_L and the V_{DD}. The V_L provides power to gate drivers for switching metal-oxide semiconductor field-effect transistor (MOSFETs), while the V_{DD} provides power for internal logic and control. Those two 1.8V regulators are powered from either the SYS or the ALT_IN input, depending on the DIS_ALT_IN bit and the V_{ALT_IN}. See the *Alternative Low-Voltage Input (ALT_IN)* section for more information.

- The SYS powers the V_L and the V_{DD} when the DIS_ALT_IN == 1 **OR** the V_{ALT_IN} is less than the switch-over voltage (V_{SWO}, typ. 2.8V).
- The ALT_IN powers the V_L and the V_{DD} when the DIS_ALT_IN == 0 **AND** the V_{ALT_IN} is greater than the V_{SWO}.

When either the I2C_EN or the ENx pin is pulled high, the MAX77540 enables bias circuitry as well as V_L and V_{DD} supplies. As soon as the V_{DD} supply becomes stable, the MAX77540 reads the R_{SELx} values for configuring the device. While both the V_{SYS} and the V_{DD} are valid, I^2C serial communication is activated. Enabling I^2C by pulling the I2C_EN pin high allows the host processor to modify configuration settings before activating the Buck outputs.

Table 1. V_{DD} and I^2C Enable Truth Table

I2C_EN (PIN)	EN1 OR EN2 (PIN)	V_{DD} AND I^2C SERIAL INTERFACE
Low	Low	Disabled
X	High	Enabled
High	X	Enabled

Alternative Low-Voltage Input (ALT_IN)

When an alternative power source (V_{ALT_IN}) is available between the switch-over voltage (V_{SWO}) and 5.5V, it can optionally be used to power the dedicated 1.8V linear regulator (V_L and V_{DD}) in order to improve the efficiency. As shown in Figure 1, the switch-over circuit dynamically selects the input of the V_L and the V_{DD} supplies between the SYS and the ALT_IN pins as needed to maintain steady operation. When the device exits Shutdown mode (I2C_EN = 1 **OR** ENx = 1), the linear regulator is initially powered from the SYS pin and it can be switched over to the ALT_IN pin if a valid power source is connected to the ALT_IN. The ALT_IN_I interrupt and the ALT_SWO status bits indicate the status of the switch-over circuit. There are three ways of using the ALT_IN input:

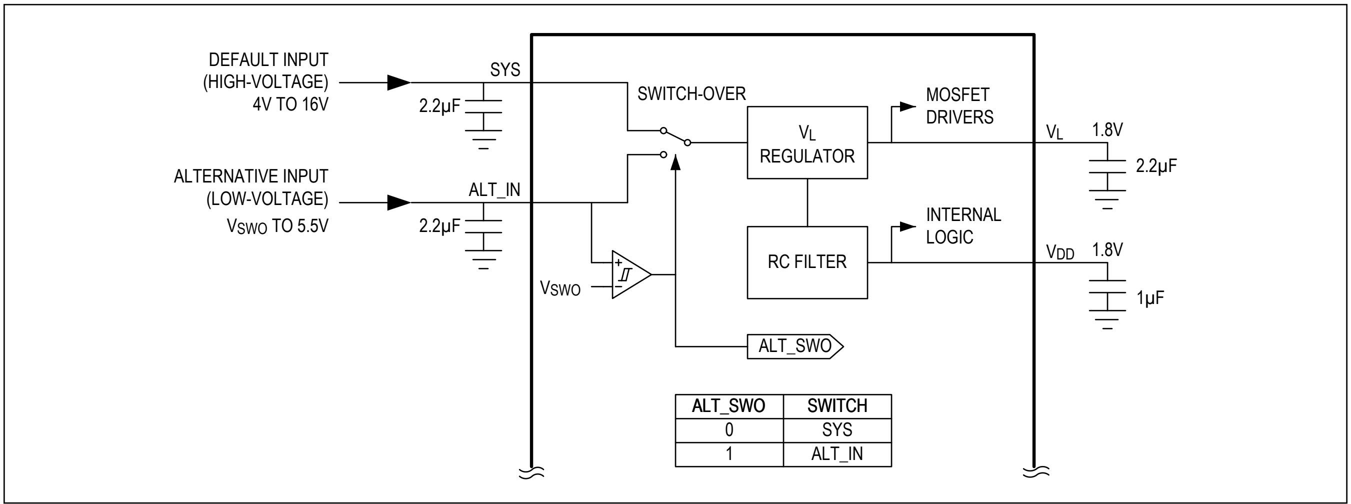


Figure 1. Alternative Input Switch-Over Circuit

- Option 1: Connect the ALT_IN pin to the AGND (not used). In this case, the internal linear regulator permanently receives power from the SYS pin.
- Option 2: Connect the ALT_IN pin to one of the Buck outputs which is greater than the V_{SWO}. Using a Buck output for powering up the linear regulator improves the total efficiency of the device (it is OK to turn the Buck output on and off dynamically).
- Option 3: Connect the ALT_IN pin to an external high-efficiency DC source greater than the V_{SWO} when neither Buck output is greater than the V_{SWO} (using a high-efficiency power source also improves the total system efficiency).

Output Enable Control

The MAX77540 has dedicated logic input pins (EN1 and EN2) for enabling individual Buck outputs. When the ENx is pulled above the V_{IH}, the corresponding Buck output is enabled. In case the MAX77540 exits Shutdown mode by the ENx, it takes about 220μs (typ) to turn on the internal bias circuitry and evaluate the R_{SELx} before propagating the Buck enable signals. To prevent chatter, the ENx pins must be driven either high or low.

The Buck outputs can also be turned on by setting the Mx_EN bits to '1' through the I^2C serial interface. The logical interaction between the enable pins (ENx) and their corresponding I^2C enable bits (Mx_EN) is 'OR'. The serial interface is active whenever the V_{DD} regulator is enabled (see Table 1).

Undervoltage Lockout

When the V_{SYS} voltage falls below the V_{UVLO_F} (typ 3.7V), the MAX77540 initiates an immediate shutdown of all individual Buck outputs. A UVLO event forces the device to a dormant state until the V_{SYS} voltage rises above the UVLO rising threshold (typ 3.9V). If the V_{SYS} voltage drops down to the power-on reset (POR) threshold (typ 1.7V), the V_{DD} supply turns off (all the registers are reset) and the MAX77540 enters into shutdown state.

Thermal Warnings and Thermal Shutdown (T_{SHDN})

The MAX77540 has two thermal warnings and a thermal shutdown (T_{SHDN}) threshold to monitor whether the junction temperature rises above +120°C and +140°C. As shown in Figure 2, the device enters thermal shutdown (T_{SHDN}) if the junction temperature exceeds the T_{SHDN} (approximately +165°C typ.). A T_{SHDN} event initiates a shutdown of all individual outputs immediately. See the *Fault Protection* section for more information. Thermal monitoring is active whenever any of the following conditions is true:

- One of the Buck outputs is enabled.
- Force temperature monitors enable bit sets (EN_FTMON = 1).
- Thermal protection is enabled (for any reason) and detects $T_J \geq 120°C$ (in this case, thermal monitoring remains active until $T_J \leq 105°C$).

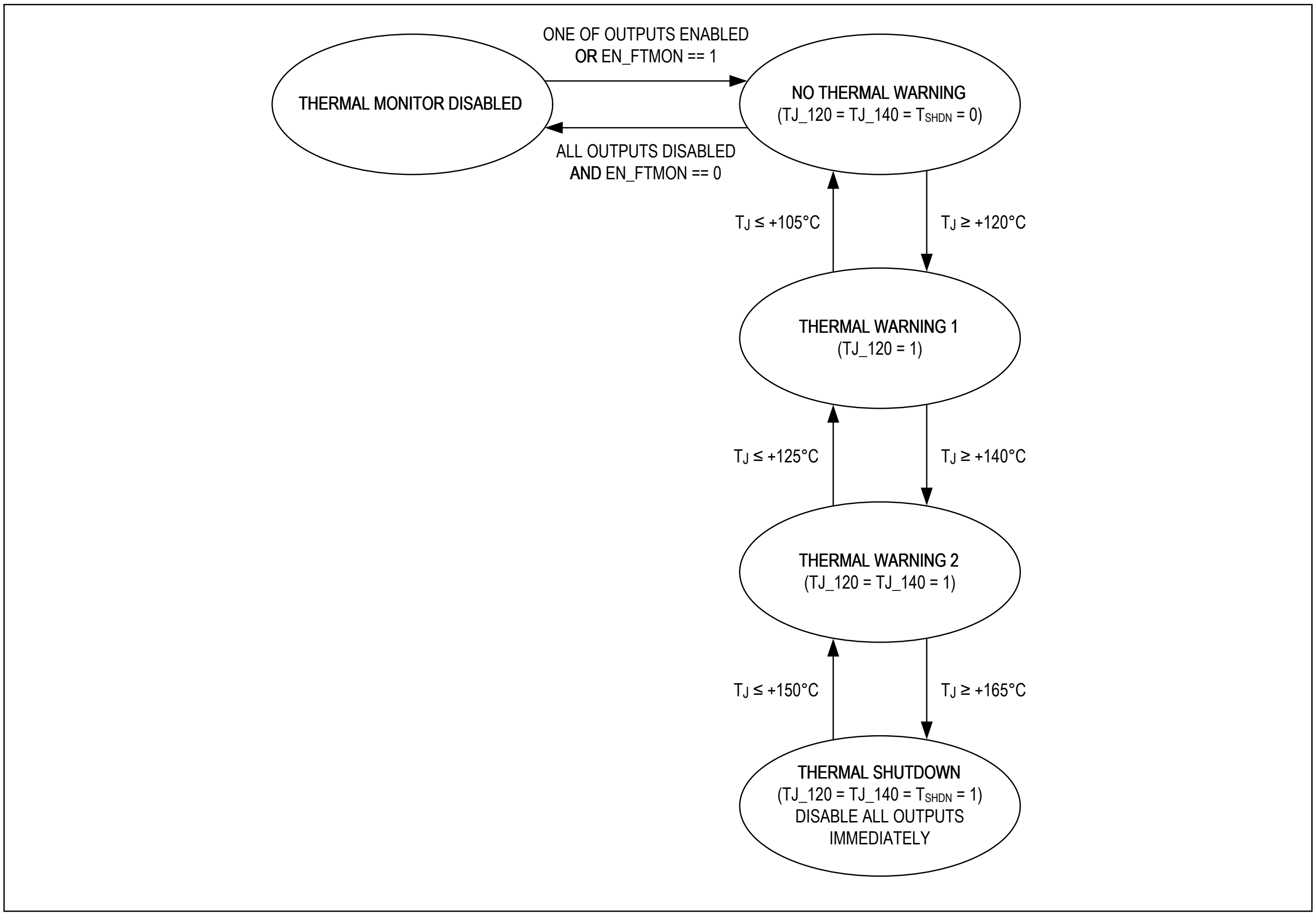


Figure 2. Thermal Monitor State Diagram

Interrupt (IRQB) and Mask

The IRQB is an active-low, open-drain output and it is for indicating to the host processor that the status on the MAX77540 has changed. The IRQB is the logical 'NOR' of all unmasked interrupt bits. See the *Register Map* for a full list of available status and interrupt bits.

The IRQB output asserts (goes low) anytime an unmasked interrupt bit is triggered. The host processor reads the interrupt source register (ADDR 0x00) and the interrupt registers that are indicated by the interrupt source register to check the cause of interrupt event. Note that the interrupt source register is cleared when the corresponding interrupt register group is read by the host processor.

All the interrupt events are edge-triggered. Therefore, the same interrupt is not generated repeatedly even though the interrupt condition persists.

Each interrupt register can be read at a time and all interrupt bits are 'Clear-on-Read' bits. The IRQB output deasserts (goes high) when all interrupt bits have been cleared. If an interrupt is captured during the read sequence, the IRQB output is held low. When the IRQB output is pulled low by an unmasked interrupt event, the IRQB output stays low until the interrupt bit is cleared by the reading operation of the host processor or the corresponding interrupt mask bit is set to ‘1’ (masked). All interrupts (except the UVLO_I) are masked by default. Masked interrupt bits do not cause the IRQB pin to assert.

Register Reset Condition

The configuration registers of the device reset to default values when the I2C_EN, the EN1, and the EN2 are all logic low or the V_{SYS} falls below its POR threshold.

Detailed Description—Dual-Phase Configurable Buck Converter

The MAX77540 is a high-efficiency, phase-configurable Buck converter with two 3A phases (Φ). Two output voltage sensing inputs allow up to two regulated outputs. Each Buck converter operates on an input supply between 4V and 16V. The output voltages are preset using the SELx inputs and further configurable with an I^2C serial interface between 0.5V and 5.2V in 5mV, 10mV, or 20mV steps depending on the Mx_RNG[1:0] bits. See the *Output Voltage Setting* section.

Each switching phase supports 3A and dual-phase (2Φ) configuration supports up to 6A. Phase configuration is user-programmable by tying the SEL2 pin to the AGND on the PCB. See the *Phase Configuration* section.

Buck Converter Control Scheme

The MAX77540 uses Maxim's proprietary adaptive constant on-time (COT) current-mode control scheme. The adaptive COT control provides fast response to load transients, inherent compensation to input voltage variation, and stable performance at low duty cycles. As shown in Figure 3, Buck1 is referenced in the following explanation.

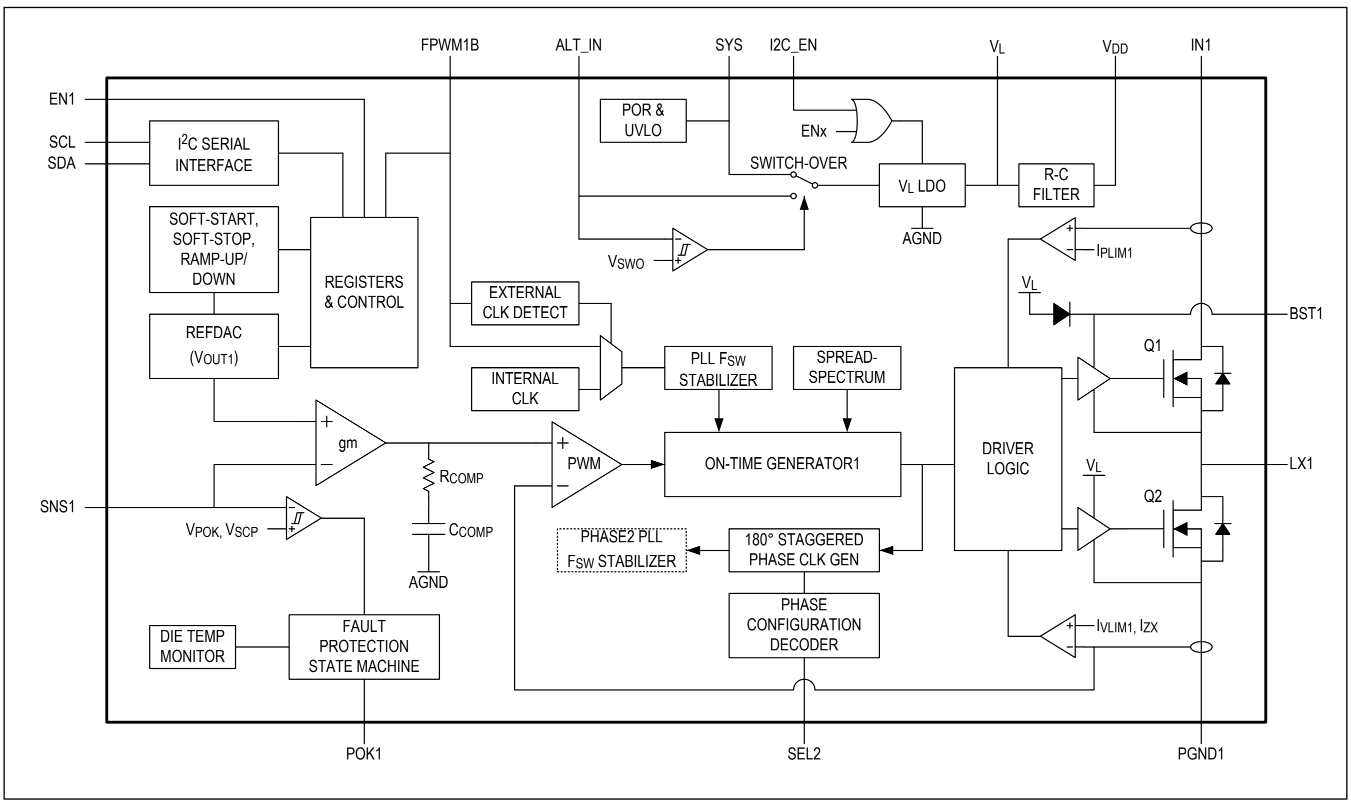


Figure 3. Functional Block Diagram

An on-time (MOSFET Q1 is on) is controlled by an on-time generator circuit and this circuit calculates an on-time based on the input voltage (V_{IN1}), the output voltage (V_{OUT1}), and the target switching frequency (F_{SW1}). An off-time (MOSFET Q2 is on) begins when the on-time ends. During the dead-time, the inductor current conducts through the intrinsic body diode. A pulse-width modulation (PWM) comparator regulates the V_{OUT1} by modulating off-time. The positive input of the PWM comparator is a voltage proportional to the actual output voltage error. The negative input is a voltage proportional to the inductor current sensed through the MOSFET Q2. The PWM comparator begins an on-time when the error voltage becomes higher than the current-sense signal. The off-time automatically begins again when the calculated on-time expires. A phase-locked loop (PLL) stabilizes the switching frequency and controls phase spacing. The PLL stabilizes Phase2 (LX2) 180° apart from Phase1 when the output is configured for the dual-phase (2Φ) operation. In dual-phase configuration, both the master and the slave phases are activated and always switch in sequence during steady-state operation. The phases do not add or shed.

Buck Operating Modes

The buck converters have three operating modes shown in Figure 4 and transitions between the modes are determined by operating conditions and mode control settings. The operating mode setting can be changed any time while I²C communication is available. Toggling between SKIP and FPWM modes is also controlled by the FPWMxB pins. Pulling the FPWMxB pin low operates the corresponding buck in forced-PWM mode. When the FPWMxB pin is held high, the operating mode is controlled by the Mx_LPM and the Mx_FPWM bits.

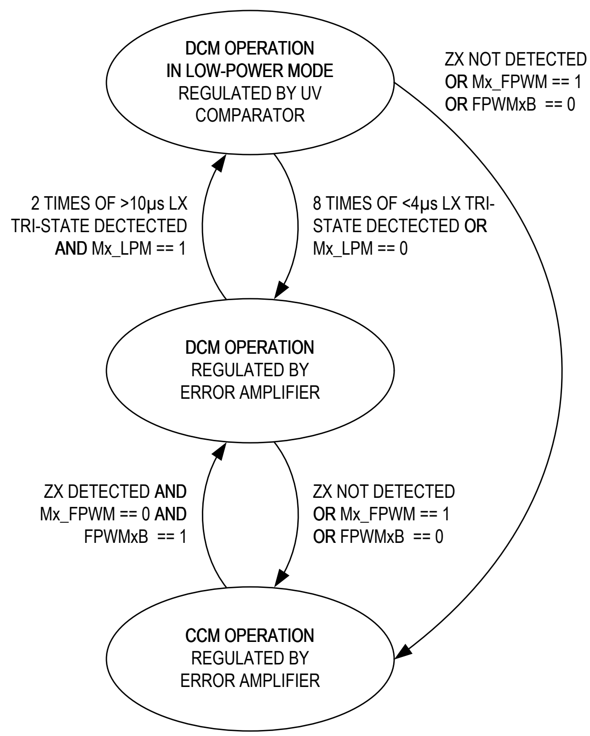


Figure 4. Buck Operating Modes

Detail mode control settings are described as follows:

SKIP Mode

In SKIP mode (*Mx_LPM == Mx_FPWM == 0* ***AND*** *FPWMxB == 1*), the buck converter operates either in discontinuous-conduction mode (DCM) or continuous-conduction mode (CCM) depending on loading. If the averaged output current is lower than a half of inductor peak-to-peak ripple current under light load condition, the low-side MOSFET turns off as soon as the inductor current drops to near zero ampere (zero-crossing). Then, the switching node (LX) remains in tri-state (Hi-Z) until the next on-time is triggered. In this way, the buck prevents a negative inductor current which results in improving light-load efficiency by reducing the total number of switching cycles needed to regulate the output voltage.

When no zero-crossing (ZX) is detected (under heavier load), the buck controller goes into CCM where the averaged output current is greater than a half of inductor ripple current. In both DCM and CCM, the output voltage is regulated by an error amplifier. In case the on-time determined by a given operating condition in high output voltage range (Mx_RNG[1:0] = 0x2) is not long enough, the on-time automatically extends until the inductor current reaches 500mA for ensuring enough off-time to detect the ZX reliably.

Low-Power SKIP (LP-SKIP) Mode

Low-Power SKIP mode (*Mx_LPM == FPWMxB == 1* ***AND*** *Mx_FPWM == 0*) is similar to SKIP mode as a negative inductor current is not allowed in LP-SKIP mode as well. When the averaged output current is decreased further down (>10μs of LX tri-state is detected two times consecutively) in SKIP mode, the buck converter enters LP-SKIP mode when Low Power mode is enabled. In LP-SKIP mode, the error amplifier and other internal blocks are deactivated to lower down I_Q consumption. Instead, a low-power comparator monitors the output voltage in LP-SKIP mode.

The Buck enters DCM operation in SKIP mode when the duration of LX tri-state is shorter than 4μs for eight times in a row, or LP-SKIP mode is disabled (*Mx_LPM == 0*). If no zero-crossing is detected (i.e., sudden load transient) or FPWM mode is enabled (*Mx_FPWM = 1* ***OR*** *FPWMxB = 0*), the Buck enters CCM directly from LP-SKIP mode.

Forced-PWM (FPWM) Mode

Forced-PWM mode (*Mx_FPWM == 1* ***OR*** *FPWMxB == 0*) ensures a continuous inductor current under all load conditions. In FPWM mode, a negative inductor current though the low-side MOSFET is allowed but the maximum current is limited to the I_{NLIM} (typ -2.9A). When the buck converters enter/exit FPWM mode by the FPWMxB inputs, there is 1ms of delay in mode transition due to 1ms of debounce timer on the FPWMxB inputs.

In case a valid external frequency is detected on the FPWMxB input, the corresponding Buck enters FPWM mode regardless of its operating mode settings. See the *Frequency Tracking (FTRAK)* section for more information.

Dropout Mode

The MAX77540 architecture allows the buck converter to operate even when the input voltage becomes very close to the target output voltage. When the headroom between the input and the output voltages reduces during operation, the buck controller tries to maintain the output voltage regulation by increasing the duty cycle. In case Buck is not able to regulate the target output voltage with the maximum duty cycle (typ 98%), it automatically extends the on-time by skipping the off-times (dropout mode). In dropout mode, the low-side MOSFET turns on occasionally in order to refresh the bootstrap circuit for driving the high-side MOSFET. See the *Bootstrap Refresh* section for more information.

Switching Frequency

The MAX77540 has three nominal switching frequency options (0.5MHz, 1.0MHz, and 1.6MHz) to support optimization of efficiency, transient responses, noise performance, and solution size. The default switching frequency of each Buck is set by the SELx input (see Table 4 and Table 5) and the switching frequencies of individual Bucks are also selectable by the Mx_FREQ[1:0] bits.

At a particular time, the switching frequency (F_{SW}) of the adaptive on-time buck converter is not fixed and heavily influenced by the instantaneous load current. More on-time pulses in a given time (higher F_{SW}) is observed as the output current increases, while fewer on-times in a given time (lower F_{SW}) is observed when the output current decreases. A valid external frequency at the FPWMxB input or enabling the internal frequency tracking feature (Mx_FTRAK = 1) stabilizes the switching frequency of the corresponding Buck in steady-state operation. See the *Frequency Tracking (FTRAK)* section for more information.

In case the on-time calculated by the given operating condition is less than the minimum on-time (typ 60ns), the buck controller regulates the output voltage by increasing the off-time. As a result, the actual switching frequency becomes slower than its nominal frequency setting. For example, the calculated duty cycle for 16V_{IN} and 0.8V_{OUT} is 5%, which gives less than 60ns of on-time at 1.0MHz of nominal switching frequency. It means the actual switching frequency under this condition is slower than 1.0MHz so that 0.5MHz of nominal switching frequency setting is recommended.

Phase Configuration

The MAX77540 has two 3A switching phases configurable into either two single-phase Bucks or one dual-phase Buck. As shown in Table 2, the Buck is configured as single-output dual-phase (2Φ) when the SEL2 is shorted to the AGND. In dual-phase (2Φ) configuration, logic I/O pins and control registers for Buck2 are deactivated so that register settings of the master phase (M1) dictate the operation of the slave phase as well.

Table 2. Phase Configuration Selection

R_{SEL1} (Ω)	R_{SEL2} (Ω)	PHASE (Φ) CONFIGURATION	NUMBER OF OUTPUTS
Any	≤ 95.3	2Φ	1
Any	≥ 200	1Φ + 1Φ	2

Also, the output voltage sensing of the buck converter is assigned based on the phase configuration setting. In dual-phase configuration, the buck controller regulates the output voltage using the SNS1 pin only (the SNS2 pin is unused). Table 3 shows how to configure the output voltage sensing pins for each phase configuration.

Table 3. Buck Output Sensing Assignment

PHASE (Φ) CONFIGURATION	PHASE ASSIGNED	BUCK NAMING CONVENTION	V_{OUT} SENSING INPUT
2Φ (1 Output)	Phase1 (M1) Phase2 (S)	Buck1 (V_{OUT1})	SNS1
1Φ + 1Φ (2 Outputs)	Phase1 (M1)	Buck1 (V_{OUT1})	SNS1
	Phase2 (M2)	Buck2 (V_{OUT2})	SNS2
(Mx): Master Phase (S): Slave Phase			

Default Output Voltage Selection (SELx)

The MAX77540 supports user-selectable default voltages of individual Buck outputs with 1% tolerance (or better) resistors. The MAX77540 evaluates the resistances between the SELx and the AGND whenever the V_{DD} regulator first turns on (exits shutdown by either the I2C_EN or the ENx pin). The decoded values of the R_{SELX} are latched until the next time the device exits shutdown mode. The SELx_LATCH[4:0] status bits reflect the latched decoded values of the R_{SELX}. See the *Register Map* for more details.

The resistance between the SEL1 and the AGND (R_{SEL1}) configures the default voltage of Buck1, while the R_{SEL2} between the SEL2 and the AGND selects Buck2 default voltage. If the SEL2 pin is tied to the AGND on the PCB (R_{SEL2} ≤ 95.3Ω), the Buck is configured as a single-output dual-phase (2Φ) converter. When the dual-phase operation is selected, the decoded resistance on the SEL1 (R_{SEL1}) sets the default output voltage (V_{OUT1}). Table 4 and Table 5 decode the default selection options for the V_{OUT1} and the V_{OUT2}, respectively. Once latched, the Mx_VOUT[7:0], the Mx_RNG[1:0], and the Mx_FREQ[1:0] bits reflect the selected options. The decoded values for R_{SELX} ≥ 115kΩ are programmable at the factory.

Table 4. Default V_{OUT1} Selection

R_{SEL1} (Ω)	TARGET V_{OUT1} (V)	V_{OUT1} RANGE	F_{SW1} (MHz)
≤ 95.3	0.50	Low	1
200	0.50	Low	0.5
309	0.60	Low	0.5
422	0.60	Low	1
536	0.65	Low	0.5
649	0.65	Low	1
768	0.72	Low	0.5
909	0.72	Low	1
1.05k	0.75	Low	0.5
1.21k	0.75	Low	1
1.40k	0.80	Low	0.5
1.62k	0.80	Low	1

Table 4. Default V_{OUT1} Selection (continued)

R_{SEL1} (Ω)	TARGET V_{OUT1} (V)	V_{OUT1} RANGE	F_{SW1} (MHz)
1.87k	0.85	Low	0.5
2.15k	0.85	Low	1
2.49k	0.90	Low	0.5
2.87k	0.90	Low	1
3.74k	1.00	Low	0.5
8.06k	1.00	Mid	1
12.4k	1.10	Low	0.5
16.9k	1.10	Mid	1
21.5k	1.20	Low	0.5
26.1k	1.20	Mid	1
30.9k	1.35	Mid	1
36.5k	1.50	Mid	1
42.2k	1.80	Mid	1
48.7k	2.00	Mid	1
56.2k	2.50	High	1
64.9k	2.80	High	1
75.0k	3.30	High	1
86.6k	3.80	High	1
100k	5.00	High	1
≥ 115k	Factory Option		

Table 5. Default V_{OUT2} Selection

R_{SEL2} (Ω)	TARGET V_{OUT2} (V)	V_{OUT2} RANGE	F_{SW2} (MHz)
≤ 95.3	N/A (2Φ Operation)		
200	0.50	Low	0.5
309	0.60	Low	0.5
422	0.60	Low	1
536	0.65	Low	0.5
649	0.65	Low	1
768	0.72	Low	0.5
909	0.72	Low	1
1.05k	0.75	Low	0.5
1.21k	0.75	Low	1
1.40k	0.80	Low	0.5
1.62k	0.80	Low	1
1.87k	0.85	Low	0.5
2.15k	0.85	Low	1
2.49k	0.90	Low	0.5
2.87k	0.90	Low	1
3.74k	1.00	Low	0.5

Table 5. Default V_{OUT2} Selection (continued)

R_{SEL2} (Ω)	TARGET V_{OUT2} (V)	V_{OUT2} RANGE	F_{SW2} (MHz)
8.06k	1.00	Mid	1
12.4k	1.10	Low	0.5
16.9k	1.10	Mid	1
21.5k	1.20	Low	0.5
26.1k	1.20	Mid	1
30.9k	1.35	Mid	1
36.5k	1.50	Mid	1
42.2k	1.80	Mid	1
48.7k	2.00	Mid	1
56.2k	2.50	High	1
64.9k	2.80	High	1
75.0k	3.30	High	1
86.6k	3.80	High	1
100k	5.00	High	1
≥ 115k	Factory Option		

Output Voltage Setting

The output voltages (V_{OUTx}) are adjustable between 0.5V and 5.2V in 5mV, 10mV, or 20mV steps depending on the Mx_RNG[1:0] bits as shown in Table 6. Note that the Mx_RNG[1:0] bits must not be changed while the corresponding Buck is enabled.

In each output voltage range, the lowest code (0x00) of the Mx_VOUT[7:0] bits represents the minimum output voltage and the target output voltage is increased by one least significant bit (LSB) step as the code increases. The maximum programmable output voltage is digitally limited to the maximum output voltage in each range even if the code increases beyond that point. The default values of the Mx_VOUT[7:0] and the Mx_RNG[1:0] bits are set by the corresponding R_{SELx} values. See the *Default Output Voltage Selection (SELx)* section for more information.

For output voltages that have overlapping ranges (i.e., 1.0V), select the desired range by trading off load transient response and the required number of output capacitors. Using the 1V output example: Use low-range for a slightly better load transient response or mid-range for a slightly worse transient response but less output capacitors. See the *Output Capacitor Selection* section for more information on required output capacitance for the different output voltage ranges.

Table 6. Buck Output Voltage Range

Mx_RNG[1:0]	V_{OUT} PROGRAMMING RANGE (V)	STEP PER LSB (mV)
0x0 (Low-range)	0.5 to 1.2	5
0x1 (Mid-range)	1.0 to 2.4	10
0x2 (High-range)	2.0 to 5.2	20

Soft-Start and Soft-Stop

The Bucks always soft-start whenever they are enabled (regardless of the ENx or I^2C command) or recovering from a fault condition. When the individual Buck is disabled by the ENx or I^2C command, the Buck always initiates soft-stop. If an SCP event occurs to a Buck output, the corresponding Buck stops switching immediately (LX node becomes Hi-Z) and the other Buck starts soft-stop in a controlled manner if enabled. For a T_{SHDN} fault event, all Bucks stop switching immediately.

The Bucks have internal ramps that control the slew rate of output voltage changes during the soft-start and the soft-stop. The soft-start and the soft-stop slew rates are individually set by the SSTRT_SR[2:0] and the SSTOP_SR[2:0] bits, respectively, and they are the global settings for all Buck phases. During the soft-start and soft-stop, the Buck automatically enters the FPWM mode regardless of operating mode settings when the Mx_FSREN bit is set to '1' (default). To support the 'prebiased' startup (startup without discharging pre-existing voltage at the output), the Mx_FSREN and the Mx_ADIS100 bits need to be set to '0' before the Buck is enabled.

The SSTRT_SR[2:0] and the SSTOP_SR[2:0] bits set the slew rates of a voltage reference to an error amplifier. When the fastest slew-rate option is selected, the actual output voltage slew rate can be slower than the target setting due to limited sourcing and the sinking current capabilities of Bucks under given circuit parameters and operating conditions. See Table 7 for more information.

Dynamic Output Voltage Scaling

Whenever a new target value is written in the Mx_VOUT[7:0] bits through I^2C while the corresponding Buck is enabled, the output voltage starts to change. The output voltage ramps up (or down) at a positive (or negative) slew rate set by the corresponding Mx_RU_SR[2:0] (or Mx_RD_SR[2:0]) bits. When the Mx_FSREN bit is set, the corresponding Buck enters FPWM mode automatically (regardless of the Mx_FPWM bit) during the output voltage ramp-down. In FPWM mode, the Buck can sink current from the C_{OUTx} to the PGNDx through the low-side MOSFET, which allows the V_{OUTx} to track the negative rate set by the Mx_RD_SR[2:0] bits.

Table 7. Mx_FSREN Effect on Buck Behavior

OPERATING MODE	Mx_FSREN	BUCK BEHAVIOR IN STEADY STATE	BUCK BEHAVIOR DURING DVS
SKIP or LP-SKIP	0	Source Only	Source Only
	1	Source Only	Source or Sink
FPWM	X	Source or Sink	Source or Sink
Note: Buck outputs (V_{OUTx}) with current sinking capability can follow negative ramp rates set by the Mx_RD_SR[2:0] or the SSTOP_SR[2:0].			

If the negative inductor current reaches the I_{NLIM} (typ -2.9A), the low-side MOSFET is turned off immediately and the Buck initiates a new on-time (high-side MOSFET turn-on). Thus, the maximum slew rate during output voltage ramp-down (or soft-stop) is limited if an effective output capacitance is very high for the selected ramp-down (or soft-stop) slew rate. The maximum output voltage slew rate is calculated by following the formula, $dV_C/dt = i_C / C$.

Output Voltage Active Discharge

Each Buck converter integrates a 100Ω active discharge resistor between the LXx and the PGNDx for discharging the output capacitor when the Buck output is disabled. For faster output voltage discharge at the end of soft-stop, a 1Ω active discharge function is added. Those two active discharge resistors are individually enabled by setting the Mx_ADIS100 and the Mx_ADIS1 bits, respectively. If both the Mx_ADIS100 and the Mx_ADIS1 are set to '1', the 1Ω active discharge is first activated for 1ms right after soft-stop is completed, and then the 100Ω active discharge is enabled until the Buck is enabled next time. In shutdown mode (I2C_EN = EN1 = EN2 = 0), the 100Ω active discharge of each Buck phase is enabled by default.

Note that the 1Ω active discharge function of the corresponding output must be disabled (Mx_ADIS1 = 0) to avoid excessive power dissipation when the falling slew-rate control feature is disabled (Mx_FSREN = 0).

Bootstrap Refresh

When the Buck is in dropout operation or it operates in SKIP (or LP-SKIP) mode under extremely light load condition, the low-side MOSFET does not turn on for a long period of time. In this case, the buck controller occasionally turns on the low-side MOSFET for about 100ns (typ) in order to charge a bootstrap circuit for driving the high-side MOSFET. The bootstrap refresh interval is set to 64μs in SKIP mode (128μs in LP-SKIP) which gives 15.6kHz (7.8kHz) of minimum switching frequency. For applications that audible range noises are critical, 'Ultrasonic' mode (Mx_ULTRA == 1) increases the minimum switching frequency to 100kHz by reducing the refresh interval to 10μs. The bootstrap refresh interval selection is shown in Table 8.

Table 8. Bootstrap Refresh Interval Selection

Mx_ULTRA	REFRESH INTERVAL	
	SKIP OR DROPOUT MODE (µs)	LP-SKIP MODE (µs)
0	64	128
1	10	10

The bootstrap refresh is also required when the buck converter starts switching. As a part of the startup procedure, the buck controller forces 15 times of refresh pulses with 4µs of interval.

Frequency Tracking (FTRAK)

The MAX77540 supports frequency tracking feature. When a valid external clock is detected on the FPWMxB input (triggers the EXT_FREQ_DET_I interrupt if unmasked), the corresponding buck converter enters FPWM mode regardless of its operating mode setting and tracks the external frequency by modulating on-times. Buck1 attempts to track the beginning of on-times to the rising edges of the external clock on the FPWM1B input, while Buck2 attempts to track the beginning of on-times to the falling edges of the external clock on the FPWM2B input.

Table 9. Mx_FTRAK Enable Truth Table

EXT_FREQ_DET	Mx_FTRAK	PLL	BUCK OPERATING MODE	NOTE
0	0	Disabled	Depends on Buck Mode Setting	No Tracking
0	1	Enabled	Depends on Buck Mode Setting	Internal Freq. Tracking
1	0	Enabled	FPWM	External Freq. Tracking
1	1	Enabled	FPWM	External Freq. Tracking

As shown in Table 9, the Bucks can also track an internal clock. When the FTRAK function is enabled (Mx_FTRAK = 1), the corresponding Buck tracks the internal PLL frequency (set by the Mx_FREQ[1:0] bits) if no valid external clock is applied. In case a valid external clock is detected while the corresponding Buck is tracking the internal PLL, it switches to the external clock tracking. The frequency window for both external and internal tracking is about ±5% of the nominal switching frequency. The frequency tracking operation is legal whenever one of the buck converters is enabled regardless of the I2C_EN pin status. The FPWM1B and the FPWM2B must be driven either low or high to prevent chattering or false tracking.

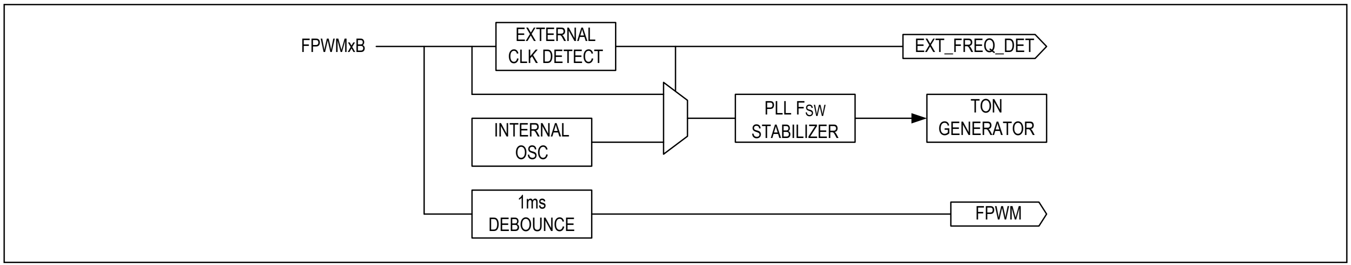


Figure 5. Frequency Tracking

Spread-Spectrum Modulation

The Bucks are capable of dithering their switching frequency for noise-sensitive applications. The spread-spectrum function of each Buck is individually enabled by setting the Mx_SS_ENV[1:0] bits. The spread-spectrum function is activated only in the CCM and it is automatically deactivated when the Bucks enter the DCM. The spread-spectrum modulation pattern is programmable either pseudorandom or triangular by the Mx_SS_PAT[1:0] bits. The spread-spectrum modulation is characterized by modulation envelope and modulation frequency:

- Modulation envelope (ΔF_{SS}) determines the maximum difference between the modulated switching frequency and the nominal switching frequency. The modulation envelope is programmable (±8%, ±12%, or ±16%) by the Mx_SS_ENV[1:0] bits and it controls 'how wide' the switching frequency dithers.

- Modulation frequency (F_{SS_MOD}) determines how often the switching frequency changes from one value to another. The modulation frequency is also programmable (1kHz, 3kHz, 5kHz, or 7kHz) by the Mx_SS_FREQ[1:0] bits and it controls 'how fast' the switching frequency dithers.

Pseudo-Random Pattern

The pseudo-random engine uses a 4-bit linear feedback shift register (LFSR) to create a pseudo-random value as shown in Figure 6. The LFSR value is converted to an analog signal and then amplified before being added to the output of the on-time generator circuit. The pseudo-random value shortens or lengthens the on-time. This causes the Buck controller to increase or decrease the switching frequency to maintain voltage regulation. Each Buck has its own pseudo-random pattern generator.

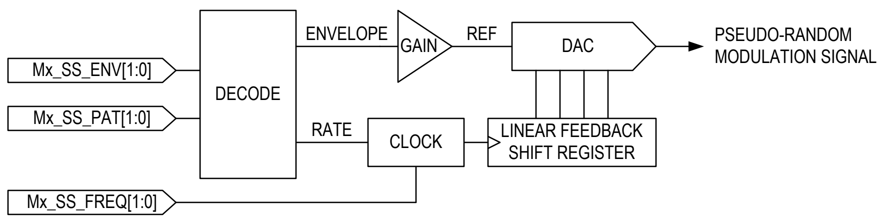


Figure 6. Pseudo-Random Modulator Engine

The modulation envelope and frequency are programmable by the Mx_SS_ENV[1:0] and the Mx_FREQ[1:0] bits. The F_{SS_MOD} sets the frequency at which the LFSR wraps back to the seed value. The clock rate of the LFSR is the F_{LFSR}. This is the frequency at which one pseudo-random value changes to another. An example is shown in Figure 7.

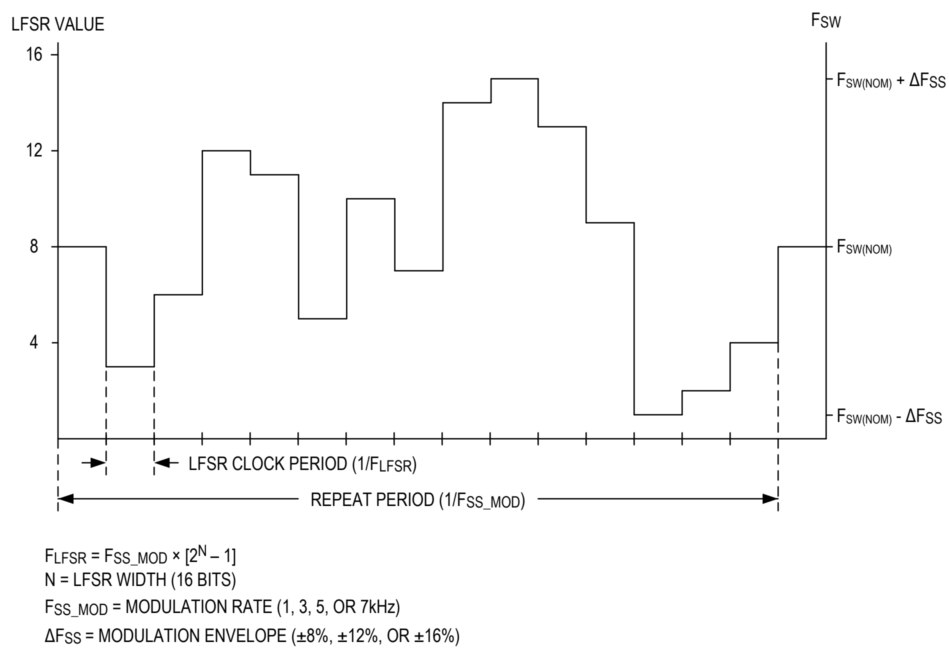


Figure 7. 4-Bit Pseudo-Random Modulation Signal Example

Triangular Pattern

The triangular engine uses a 4-bit up/down synchronous counter to create a stepped triangle pattern as shown in Figure

8. The counter value is converted to an analog signal and then amplified before being added to the output of the on-time generator circuit. The counter value progressively shortens and lengthens the on-time. This causes the Buck controller to progressively increase and decrease the switching frequency to maintain voltage regulation. Each Buck has its own triangular pattern generator.

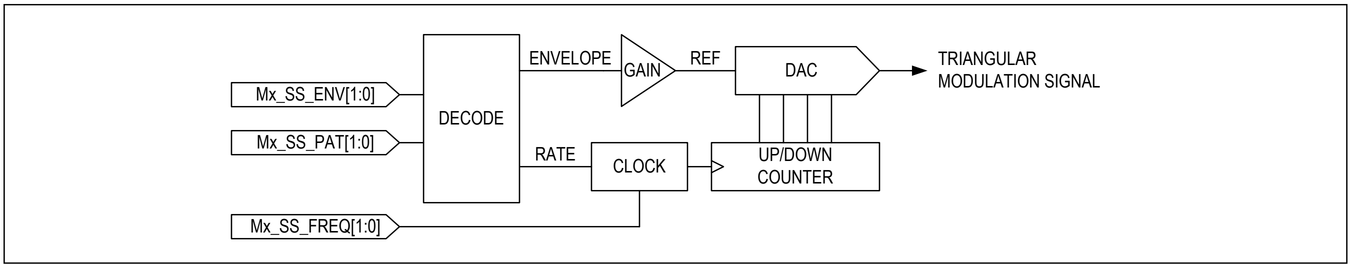


Figure 8. Triangular Modulator Engine

The modulation envelope and frequency are programmable by the Mx_SS_ENV[1:0] and the Mx_FREQ[1:0] bits. The F_{SS_MOD} sets the frequency at which the counter returns to the same value. The clock rate of the counter is the F_{COUNT}. This is the frequency at which the frequency changes from one value to another. An example is shown in Figure 9.

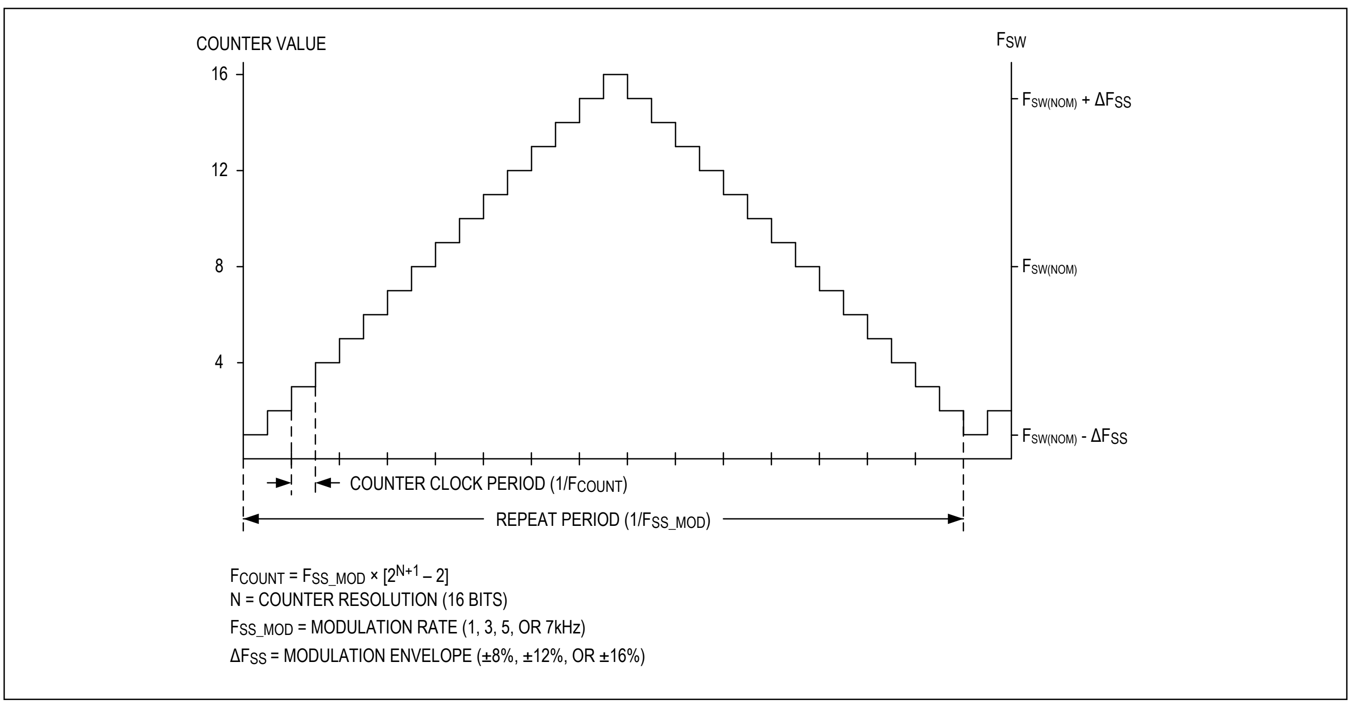


Figure 9. 4-Bit Triangular Modulation Signal Example

Inductor Current Limits

The MAX77540 has a cycle-by-cycle current limit feature that prevents the inductor current (in each phase) from increasing beyond the I_{PLIM}. If an on-time is ended by the peak current limit, the Buck prevents a new on-time from starting until the inductor current falls below the valley current limit (I_{VLIM}) which is typically set 1A less than the I_{PLIM}. This prevents the inductor current from increasing uncontrollably due to the overloaded output. In case the on-time determined by the given operating condition is less than 130ns (typ), the next on-time pulse is not triggered until the inductor current hits the I_{VLIM}. Each Buck has four PLIM thresholds which are individually set by Mx_ILIM[1:0] bits. See the Register Map for more details. The programmable PLIM thresholds allow an optimal circuit protection and inductor selections for the given operating conditions and load requirements.

Power-OK (POK)

The MAX77540 features the Power-OK (POK) comparators to monitor the quality of each Buck output. The Mx_POK status bits continuously reflect the status of these monitors. The quality of Buck output can be directly monitored by the corresponding POKx pins. The POKx are active-high, open-drain outputs that require an external pullup resistor (typ 10kΩ to 100kΩ). The POKx output goes high if the corresponding Buck output voltage rises above the V_{POK_R} (typ 82% of the V_{OUT} target) when the soft-start is completed. When the corresponding Buck falls below the V_{POK_F} (typ 78% of the V_{OUT} target), the POKx output goes low.

The Mx_POKFLT_I interrupt is also available to signal whenever any of the Mx_POK status bit changes from 1 to 0. Each Mx_POKFLT_I bit is individually maskable. See the Register Map for more details.

Fault Protection

The MAX77540 has fault protection scheme designed to protect itself from abnormal conditions. The Bucks have additional short-circuit protection (SCP) and thermal shutdown (T_{SHDN}) protection functions that operate according to the state machine in Figure 10. The operation of the state machine is summarized as follows:

- If one of the enabled Buck outputs falls below the V_{POK_F} (typ 78% of regulation target), then the Mx_POKFLT_I asserts.
- If one of the enabled Buck outputs stays below the V_{POK_R} (typ 82% of regulation target) for longer than t_{POK_TO}, then the corresponding output is disabled immediately, while other outputs initiate soft-stop.
- If one of the phases continues to have an unbroken string of on-times terminated by current limit for longer than the t_{POK_TO}, then the corresponding output is disabled immediately, while other outputs initiate soft-stop (the Mx_SCPFLT_I interrupt asserts when unmasked).
- If one of the enabled Buck outputs falls below the V_{SCP} (typ 20% of regulation target), then the corresponding output is disabled immediately, while other outputs initiate soft-stop.
- If the junction temperature exceeds the T_{SHDN} (typ 165°C), then all Bucks outputs are disabled immediately and the TSHDN_I interrupt asserts.
- The POK and SCP monitoring is not active during the soft-start and soft-stop.

To exit the fault state, all of the following conditions need to be satisfied:

- The die temperature falls below the T_{SHDN} by approximately 15°C (T_{SHDN} = 0).
- One or all Bucks are disabled:
  - If the fault state was latched due to SCP, then only the Buck that caused SCP needs to be disabled to clear fault.
  - If the fault state was latched due to T_{SHDN}, then all Buck outputs need to be disabled to clear fault.

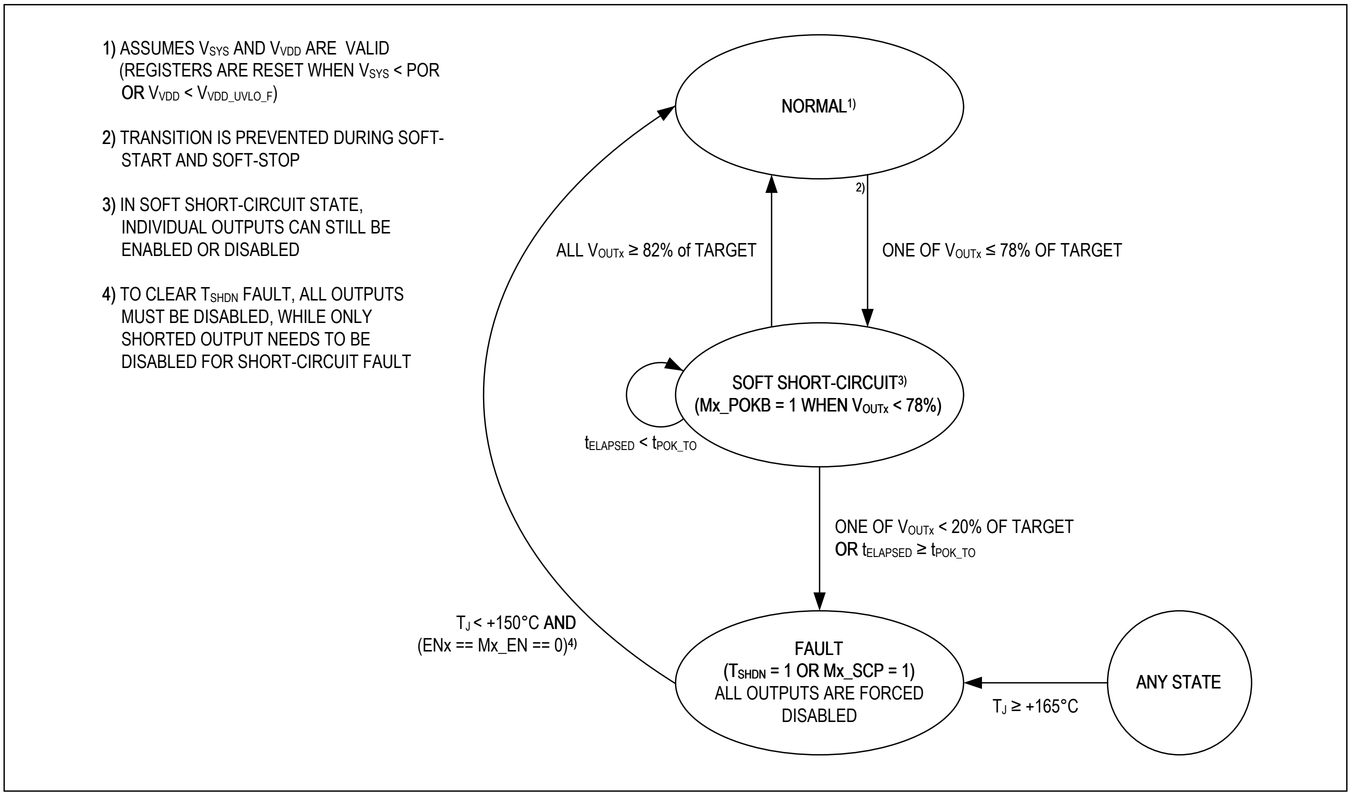


Figure 10. Fault Protection State Diagram

Detailed Description—I²C Serial Interface

The MAX77540 features an I²C version 3.0 compatible, 2-wire serial interface consisting of a serial clock line (SCL) and a bidirectional serial data line (SDA). The MAX77540 is a slave-only device that relies on an external bus master to generate the SCL clock. The SCL clock rates from 0Hz to 3.4MHz are supported. As I²C is an open-drain bus, the SDA and the SCL require external pullup resistors.

Slave Address

The I²C communication controller implements a 7-bit slave addressing and the slave address is user-selectable using ADDR pin on the PCB. All other slave addresses not listed in Table 10 are not acknowledged. The device uses 8-bit registers with 8-bit register addressing. They support standard communication protocols: (1) Writing to a single register, (2) Writing to multiple sequential registers with an autoincrement data pointer, (3) Reading from a single register, and (4) Reading from multiple sequential registers with an autoincrement data pointer. For additional information about I²C protocols, refer to I²C specifications.

Table 10. I²C Slave Address Options

ADDR PIN	7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
0V	7'h75 (111 0101)	0xEA (1110 1010)	0xEB (1110 1011)
V_{DD}	7'h76 (111 0110)	0xEC (1110 1100)	0xED (1110 1101)
FLOAT	7'h77 (111 0111)	0xEE (1110 1110)	0xEF (1110 1111)

Register Map

MAX77540 WLP Package

ADDRESS	NAME	MSB							LSB
GLOBAL CONFIGURATION 1									
0x00	INT_SRC[7:0]	RESERVED[5:0]						BUCK_I	TOPSYS_I
0x01	INT_SRC_M[7:0]	RESERVED[5:0]						BUCK_M	TOPSYS_M
0x02	TOPSYS_INT[7:0]	RESERVED[1:0]		EXT_FREQ_DET_I	ALT_SWO_I	UVLO_I	TSHDN_I	TJ_140C_I	TJ_120C_I
0x03	TOPSYS_INT_M[7:0]	RESERVED[1:0]		EXT_FREQ_DET_M	ALT_SWO_M	UVLO_M	TSHDN_M	TJ_140C_M	TJ_120C_M
0x04	TOPSYS_STAT[7:0]	RESERVED[1:0]		EXT_FREQ_DET	ALT_SWO	UVLO	TSHDN	TJ_140	TJ_120
0x06	DEVICE_CFG1[7:0]	RESERVED[2:0]			SEL1_LATCH[4:0]				
0x07	DEVICE_CFG2[7:0]	RESERVED[2:0]			SEL2_LATCH[4:0]				
0x08	TOPSYS_CFG[7:0]	RESERVED[4:0]					RESERVED	RESERVED	DIS_ALT_IN
0x09	PROT_CFG[7:0]	RESERVED[4:0]					EN_FTMON	POK_TO[1:0]	
0x0B	EN_CTRL[7:0]	RESERVED[1:0]		M2_LPM	M1_LPM	RESERVED[1:0]		M2_EN	M1_EN
GLOBAL CONFIGURATION 2									
0x11	GLB_CFG1[7:0]	RESERVED[1:0]		SSTOP_SR[2:0]			SSTRT_SR[2:0]		
BUCK1 CONFIGURATION									
0x20	BUCK_INT[7:0]	RESERVED[1:0]		M2_SCFLT_I	M1_SCFLT_I	RESERVED[1:0]		M2_POKFLT_I	M1_POKFLT_I
0x21	BUCK_INT_M[7:0]	RESERVED[1:0]		M2_SCFLT_M	M1_SCFLT_M	RESERVED[1:0]		M2_POKFLT_M	M1_POKFLT_M
0x22	BUCK_STAT[7:0]	RESERVED[1:0]		M2_SCFLT	M1_SCFLT	RESERVED[1:0]		M2_POK	M1_POK
0x23	M1_VOUT[7:0]	M1_VOUT[7:0]							
0x25	M1_CFG1[7:0]	M1_RNG[1:0]		M1_RD_SR[2:0]			M1_RU_SR[2:0]		
0x26	M1_CFG2[7:0]	M1_SS_ENV[1:0]		M1_SS_FREQ[1:0]		M1_SS_PAT[1:0]		M1_FSREN	M1_FPWM
0x27	M1_CFG3[7:0]	M1_ADIS100	M1_ADIS1	M1_ULTRA	M1_FTRAK	M1_FREQ[1:0]		M1_ILIM[1:0]	
BUCK2 CONFIGURATION									
0x33	M2_VOUT[7:0]	M2_VOUT[7:0]							
0x35	M2_CFG1[7:0]	M2_RNG[1:0]		M2_RD_SR[2:0]			M2_RU_SR[2:0]		
0x36	M2_CFG2[7:0]	M2_SS_ENV[1:0]		M2_SS_FREQ[1:0]		M2_SS_PAT[1:0]		M2_FSREN	M2_FPWM
0x37	M2_CFG3[7:0]	M2_ADIS100	M2_ADIS1	M2_ULTRA	M2_FTRAK	M2_FREQ[1:0]		M2_ILIM[1:0]	

Register Details

INT_SRC (0x00)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[5:0]						BUCK_I	TOPSYS_I
Reset	0x0						0x0	0x0
Access Type	Read Only						Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:2	Reserved. Returns '0'	
BUCK_I	1	Buck Interrupt Source	0x0 = Interrupt event in Buck has not detected 0x1 = Interrupt event in Buck has detected
TOPSYS_I	0	Top-Level Interrupt Source	0x0 = Interrupt event in TOPSYS has not detected 0x1 = Interrupt event in TOPSYS has detected

INT_SRC_M (0x01)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[5:0]						BUCK_M	TOPSYS_M
Reset	0x3F						0x1	0x0
Access Type	Write, Read						Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:2	Reserved. Returns '1'	
BUCK_M	1	Buck Interrupt Source Mask	0x0 = Enable BUCK_I 0x1 = Mask BUCK_I
TOPSYS_M	0	Top-Level Interrupt Source Mask	0x0: Enable TOPSYS_I 0x1: Mask TOPSYS_I

TOPSYS_INT (0x02)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		EXT_FREQ_DET_I	ALT_SWO_I	UVLO_I	TSHDN_I	TJ_140C_I	TJ_120C_I
Reset	0x0		0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All		Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns '0'	
EXT_FREQ_DET_I	5	External Clock Frequency Detection Interrupt	0x0 = Valid external frequency has not detected at one of FPWMxB inputs 0x1= Valid external frequency has detected at one of FPWMxB inputs

BITFIELD	BITS	DESCRIPTION	DECODE
ALT_SWO_I	4	Alternate Input Switch-Over Interrupt	0x0 = Input voltage of internal bias circuitry has not switched to ALT_IN input 0x1 = Input voltage of internal bias circuitry has switched to ALT_IN input
UVLO_I	3	SYS Undervoltage Lock-Out Interrupt	0x0 = Input voltage (V_{SYS}) has not dropped below UVLO threshold 0x1 = Input voltage (V_{SYS}) has dropped below UVLO threshold
TSHDN_I	2	Thermal Shutdown Interrupt	0x0 = Junction temperature has not risen above TSHDN threshold (165°C) 0x1 = Junction temperature has risen above TSHDN threshold (165°C)
TJ_140C_I	1	Thermal Warning2 Interrupt	0x0 = Junction temperature has not risen above 140°C 0x1 = Junction temperature has risen above 140°C
TJ_120C_I	0	Thermal Warning1 Interrupt	0x0 = Junction temperature has not risen above 120°C 0x1 = Junction temperature has risen above 120°C

TOPSYS_INT_M (0x03)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		EXT_FREQ_DET_M	ALT_SWO_M	UVLO_M	TSHDN_M	TJ_140C_M	TJ_120C_M
Reset	0x3		0x1	0x1	0x0	0x1	0x1	0x1
Access Type	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns '1'	
EXT_FREQ_DET_M	5	External Clock Frequency Detection Interrupt Mask	0x0 = Enable EXT_FREQ_DET_I 0x1 = Mask EXT_FREQ_DET_I
ALT_SWO_M	4	Alternate Input Switch-Over Interrupt Mask	0x0 = Enable ALT_SWO_I 0x1 = Mask ALT_SWO_I
UVLO_M	3	SYS Undervoltage Lock-Out Interrupt Mask	0x0 = Enable UVLO_I 0x1 = Mask UVLO_I
TSHDN_M	2	Thermal Shutdown Interrupt Mask	0x0 = Enable TSHDN_I 0x1 = Mask TSHDN_I
TJ_140C_M	1	Thermal Warning2 Interrupt Mask	0x0 = Enable TJ_140C_I 0x1 = Mask TJ_140C_I
TJ_120C_M	0	Thermal Warning1 Interrupt Mask	0x0 = Enable TJ_120C_I 0x1 = Mask TJ_120C_I

TOPSYS_STAT (0x04)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		EXT_FREQ_DET	ALT_SWO	UVLO	TSHDN	TJ_140	TJ_120
Reset	0x0		0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Only		Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns '0'	
EXT_FREQ_DET	5	External Clock Frequency Detection Status	0x0 = Valid external frequency is not detected 0x1 = Valid external frequency is detected
ALT_SWO	4	Alternate Input Switch-Over Status	0x0 = V_{DD} & V_L LDO is powered from SYS 0x1 = V_{DD} & V_L LDO is powered from ALT_IN
UVLO	3	SYS Undervoltage Lock-Out Status	0x0 = $V_{SYS} \geq V_{UVLO\_R}$ 0x1 = $V_{SYS} \leq V_{UVLO\_F}$
TSHDN	2	Thermal Shutdown Status	0x0 = $T_J \leq 150°C$ 0x1 = $T_J \geq 165°C$
TJ_140	1	Thermal Warning2 Status	0x0 = $T_J \leq 125°C$ 0x1 = $T_J \geq 140°C$
TJ_120	0	Thermal Warning1 Status	0x0 = $T_J \leq 105°C$ 0x1 = $T_J \geq 120°C$

DEVICE_CFG1 (0x06)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			SEL1_LATCH[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	DESCRIPTION
RESERVED	7:5	Reserved. Returns '0'
SEL1_LATCH	4:0	SEL1 Latched Code

DEVICE_CFG2 (0x07)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[2:0]			SEL2_LATCH[4:0]				
Reset	0x0			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	DESCRIPTION
RESERVED	7:5	Reserved. Returns '0'
SEL2_LATCH	4:0	SEL2 Latched Code

TOPSYS_CFG (0x08)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[4:0]					RESERVED	RESERVED	DIS_ALT_IN
Reset	0x0					0x0	0x0	0x0
Access Type	Write, Read					Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:3	Reserved. Returns '0'	
RESERVED	2	Reserved. Returns '0'	
RESERVED	1	Reserved. Returns '0'	
DIS_ALT_IN	0	Alternative Input for V_{DD} and V_L LDO	0x0 = Allow V_{DD} and V_L supply switch over to ALT_IN 0x1 = V_{DD} and V_L LDO is powered from SYS

PROT_CFG (0x09)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[4:0]					EN_FTMON	POK_TO[1:0]	
Reset	0x0					0x0	0x0	
Access Type	Write, Read					Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:3	Reserved. Returns '0'	
EN_FTMON	2	Forced Junction Temperature Monitor	0x0 = Monitor junction temperature only when one or more outputs is/are enabled 0x1 = Monitor junction temperature even when all the outputs are disabled
POK_TO	1:0	Power-OK Fault Time-Out Setting	0x0 = Disabled 0x1 = 25ms 0x2 = 50ms 0x3 = 100ms

EN_CTRL (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M2_LPM	M1_LPM	RESERVED[1:0]		M2_EN	M1_EN
Reset	0x0		0x0	0x0	0x0		0x0	0x0
Access Type	Write, Read		Write, Read	Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns '0'	
M2_LPM	5	Buck Master2 Low Power Mode Control	0x0 = Disable 0x1 = Enable
M1_LPM	4	Buck Master1 Low Power Mode Control	0x0 = Disable 0x1 = Enable

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	3:2	Reserved. Returns '0'	
M2_EN	1	Buck Master2 Enable Control	0x0 = Disable 0x1 = Enable (‘OR’ Logic with EN2 Input)
M1_EN	0	Buck Master1 Enable Control	0x0 = Disable 0x1 = Enable (‘OR’ Logic with EN1 Input)

GLB_CFG1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		SSTOP_SR[2:0]			SSTRT_SR[2:0]		
Reset	0x0		0x0			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns '0'	
SSTOP_SR	5:3	Global Soft-Stop Slew-Rate Control	0x0 = -0.15mV/μs 0x1 = -0.625mV/μs 0x2 = -1.25mV/μs 0x3 = -2.5mV/μs 0x4 = -5.0mV/μs 0x5 = -10mV/μs 0x6 = -20mV/μs 0x7 = -40mV/μs
SSTRT_SR	2:0	Global Soft-Start Slew-Rate Control	0x0 = 0.15mV/μs 0x1 = 0.625mV/μs 0x2 = 1.25mV/μs 0x3 = 2.5mV/μs 0x4 = 5.0mV/μs 0x5 = 10mV/μs 0x6 = 20mV/μs 0x7 = 40mV/μs

BUCK_INT (0x20)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M2_SCFLT_I	M1_SCFLT_I	RESERVED[1:0]		M2_POKFLT_I	M1_POKFLT_I
Reset	0x0		0x0	0x0	0x0		0x0	0x0
Access Type	Read Clears All		Read Clears All	Read Clears All	Read Clears All		Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns '0'	
M2_SCFLT_I	5	Buck Master2 Short-Circuit Fault Interrupt	0x0 = Buck Master2 Short-circuit Fault has not been detected 0x1 = Buck Master2 Short-circuit Fault has been detected

BITFIELD	BITS	DESCRIPTION	DECODE
M1_SCFLT_I	4	Buck Master1 Short-Circuit Fault Interrupt	0x0 = Buck Master1 Short-circuit Fault has not been detected 0x1 = Buck Master1 Short-circuit Fault has been detected
RESERVED	3:2	Reserved. Returns '0'	
M2_POKFLT_I	1	Buck Master2 Power-OK Fault Interrupt	0x0 = Buck Master2 Power-OK Fault has not been detected 0x1 = Buck Master2 Power-OK Fault has not been detected
M1_POKFLT_I	0	Buck Master1 Power-OK Fault Interrupt	0x0 = Buck Master1 Power-OK Fault has not been detected 0x1 = Buck Master1 Power-OK Fault has been detected

BUCK_INT_M (0x21)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M2_SCFLT_M	M1_SCFLT_M	RESERVED[1:0]		M2_POKFLT_M	M1_POKFLT_M
Reset	0x3		0x1	0x1	0x3		0x1	0x1
Access Type	Write, Read		Write, Read	Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns '1'	
M2_SCFLT_M	5	Buck Master2 Short-Circuit Fault Interrupt Mask	0x0 = Enable M2_SCFLT_I 0x1 = Mask M2_SCFLT_I
M1_SCFLT_M	4	Buck Master1 Short-Circuit Fault Interrupt Mask	0x0 = Enable M1_SCFLT_I 0x1 = Mask M1_SCFLT_I
RESERVED	3:2	Reserved. Returns '1'	
M2_POKFLT_M	1	Buck Master2 Power-OK Fault Interrupt Mask	0x0 = Enable M2_POKFLT_I 0x1 = Mask M2_POKFLT_I
M1_POKFLT_M	0	Buck Master1 Power-OK Fault Interrupt Mask	0x0 = Enable M1_POKFLT_I 0x1 = Mask M1_POKFLT_I

BUCK_STAT (0x22)

BIT	7	6	5	4	3	2	1	0
Field	RESERVED[1:0]		M2_SCFLT	M1_SCFLT	RESERVED[1:0]		M2_POK	M1_POK
Reset	0x0		0x0	0x0	0x0		0x0	0x0
Access Type	Read Only		Read Only	Read Only	Read Only		Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7:6	Reserved. Returns '0'	
M2_SCFLT	5	Buck Master2 Short-Circuit Fault Status	0x0 = Buck Master2 output voltage is higher than its SCP threshold, or Buck Master2 is disabled 0x1 = Buck Master2 output voltage is lower than its SCP threshold

BITFIELD	BITS	DESCRIPTION	DECODE
M1_SCFLT	4	Buck Master1 Short-Circuit Fault Status	0x0 = Buck Master1 output voltage is higher than its SCP threshold, or Buck Master1 is disabled 0x1 = Buck Master1 output voltage is lower than its SCP threshold
RESERVED	3:2	Reserved. Returns '0'	
M2_POK	1	Buck Master2 Power-OK Status	0x0 = Buck Master2 output voltage is lower than its POK threshold, or Buck Master2 is disabled 0x1 = Buck Master2 output voltage is higher than its POK threshold
M1_POK	0	Buck Master1 Power-OK Status	0x0 = Buck Master1 output voltage is lower than its POK threshold, or Buck Master1 is disabled 0x1 = Buck Master1 output voltage is higher than its POK threshold

M1_VOUT (0x23)

BIT	7	6	5	4	3	2	1	0
Field	M1_VOUT[7:0]							
Reset	0x41							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
M1_VOUT	7:0	Buck Master1 Output Voltage Control Register	When M1_RNG = 0x0: 0x0 - 0x8B = (0.5 + 0.005 x M1_VOUT)V 0x8C - 0xFF = 1.20V When M1_RNG = 0x1: 0x0 - 0x8B = (1.0 + 0.01 x M1_VOUT)V 0x8C - 0xFF = 2.40V When M1_RNG = 0x2: 0x0 - 0x9F = (2.0 + 0.02 x M1_VOUT)V 0xA0 - 0xFF = 5.20V

M1_CFG1 (0x25)

BIT	7	6	5	4	3	2	1	0
Field	M1_RNG[1:0]		M1_RD_SR[2:0]			M1_RU_SR[2:0]		
Reset	0x2		0x0			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
M1_RNG	7:6	Buck Master1 Output Voltage Range Setting (Register setting must not be changed while the output is enabled)	0x0 = Low-range (0.5V to 1.2V, 5mV step) 0x1 = Mid-range (1.0V to 2.4V, 10mV step) 0x2 = High-range (2.0V to 5.2V, 20mV step) 0x3 = Reserved

BITFIELD	BITS	DESCRIPTION	DECODE
M1_RD_SR	5:3	Buck Master1 Ramp-Down Slew-Rate Setting	0x0 = -0.15mV/µs 0x1 = -0.625mV/µs 0x2 = -1.25mV/µs 0x3 = -2.5mV/µs 0x4 = -5.0mV/µs 0x5 = -10mV/µs 0x6 = -20mV/µs 0x7 = -40mV/µs
M1_RU_SR	2:0	Buck Master1 Ramp-Up Slew-Rate Setting	0x0 = 0.15mV/µs 0x1 = 0.625mV/µs 0x2 = 1.25mV/µs 0x3 = 2.5mV/µs 0x4 = 5.0mV/µs 0x5 = 10mV/µs 0x6 = 20mV/µs 0x7 = 40mV/µs

M1_CFG2 (0x26)

BIT	7	6	5	4	3	2	1	0
Field	M1_SS_ENV[1:0]		M1_SS_FREQ[1:0]		M1_SS_PAT[1:0]		M1_FSREN	M1_FPWM
Reset	0x0		0x0		0x3		0x1	0x0
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
M1_SS_ENV	7:6	Buck Master1 Spread Spectrum Envelope Setting	0x0 = Disable 0x1 = ±8% 0x2 = ±12% 0x3 = ±16%
M1_SS_FREQ	5:4	Buck Master1 Spread Spectrum Frequency Setting	0x0 = 1kHz 0x1 = 3kHz 0x2 = 5kHz 0x3 = 7kHz
M1_SS_PAT	3:2	Buck Master1 Spread Spectrum Pattern Setting	0x0 = Triangular Pattern (0001b to 1111b) 0x1 = Pseudo-Random Polynomial (x4 + x + 1) 0x2 = Pseudo-Random Polynomial (x4 + x3 + 1) 0x3 = Pseudo-Random Polynomial (Alternating "x4 + x + 1" and "x4 + x3 + 1" every cycle)
M1_FSREN	1	Buck Master1 Falling Slew-rate Control	0x0 = Disable (Buck does not sink current from C_{OUT} in SKIP or LP-SKIP mode) 0x1 = Enable (Buck operates in FPWM mode to sink current from C_{OUT} when its $V_{OUT(TARGET)}$ is lower than the actual V_{OUT})
M1_FPWM	0	Buck Master1 Forced-PWM Control	0x0 = Disable (Automatic SKIP mode operation under light load condition) 0x1 = Enable (‘OR’ Logic with FPWM1B input)

M1_CFG3 (0x27)

BIT	7	6	5	4	3	2	1	0
Field	M1_ADIS100	M1_ADIS1	M1_ULTRA	M1_FTRAK	M1_FREQ[1:0]		M1_ILIM[1:0]	
Reset	0x1	0x0	0x0	0x0	0x1		0x3	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
M1_ADIS100	7	Buck Master1 100Ω Active Discharge	0x0 = Disable 0x1 = Enable
M1_ADIS1	6	Buck Master1 1Ω Active Discharge, Note that 1Ω active discharge must be disabled when falling slew-rate function of corresponding output is disabled (M1_FSREN = 0)	0x0 = Disable 0x1 = Enable (Active for 1ms after Soft-stop is completed)
M1_ULTRA	5	Buck Master1 Ultrasonic Mode Control	0x0 = Disable 0x1 = Enable
M1_FTRAK	4	Buck Master1 Internal Frequency Tracking Control	0x0 = Disable 0x1 = Enable
M1_FREQ	3:2	Buck Master1 Switching Frequency Setting	0x0 = 0.5MHz 0x1 = 1.0MHz 0x2 = 1.6MHz 0x3 = 1.6MHz
M1_ILIM	1:0	Buck Master1 Peak Current Limit Setting	0x0 = 1.50A 0x1 = 2.25A 0x2 = 3.00A 0x3 = 4.50A

M2_VOUT (0x33)

BIT	7	6	5	4	3	2	1	0
Field	M2_VOUT[7:0]							
Reset	0x96							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
M2_VOUT	7:0	Buck Master2 Output Voltage Control Register	When M2_RNG = 0x0: 0x0 - 0x8B = (0.5 + 0.005 x M2_VOUT)V 0x8C - 0xFF = 1.20V When M2_RNG = 0x1: 0x0 - 0x8B = (1.0 + 0.01 x M2_VOUT)V 0x8C - 0xFF = 2.40V When M2_RNG = 0x2: 0x0 - 0x9F = (2.0 + 0.02 x M2_VOUT)V 0xA0 - 0xFF = 5.20V

M2_CFG1 (0x35)

BIT	7	6	5	4	3	2	1	0
Field	M2_RNG[1:0]		M2_RD_SR[2:0]			M2_RU_SR[2:0]		
Reset	0x2		0x0			0x4		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
M2_RNG	7:6	Buck Master2 Output Voltage Range Setting (Register setting must not be changed while the output is enabled)	0x0 = Low-range (0.5V to 1.2V, 5mV step) 0x1 = Mid-range (1.0V to 2.4V, 10mV step) 0x2 = High-range (2.0V to 5.2V, 20mV step) 0x3 = Reserved
M2_RD_SR	5:3	Buck Master2 Ramp-Down Slew-Rate Setting	0x0 = -0.15mV/μs 0x1 = -0.625mV/μs 0x2 = -1.25mV/μs 0x3 = -2.5mV/μs 0x4 = -5.0mV/μs 0x5 = -10mV/μs 0x6 = -20mV/μs 0x7 = -40mV/μs
M2_RU_SR	2:0	Buck Master2 Ramp-Up Slew-Rate Setting	0x0 = 0.15mV/μs 0x1 = 0.625mV/μs 0x2 = 1.25mV/μs 0x3 = 2.5mV/μs 0x4 = 5.0mV/μs 0x5 = 10mV/μs 0x6 = 20mV/μs 0x7 = 40mV/μs

M2_CFG2 (0x36)

BIT	7	6	5	4	3	2	1	0
Field	M2_SS_ENV[1:0]		M2_SS_FREQ[1:0]		M2_SS_PAT[1:0]		M2_FSREN	M2_FPWM
Reset	0x0		0x0		0x3		0x1	0x0
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
M2_SS_ENV	7:6	Buck Master2 Spread Spectrum Envelope Setting	0x0 = Disable 0x1 = ±8% 0x2 = ±12% 0x3 = ±16%
M2_SS_FREQ	5:4	Buck Master2 Spread Spectrum Frequency Setting	0x0 = 1kHz 0x1 = 3kHz 0x2 = 5kHz 0x3 = 7kHz
M2_SS_PAT	3:2	Buck Master2 Spread Spectrum Pattern Setting	0x0 = Triangular Pattern (0001b to 1111b) 0x1 = Pseudo-Random Polynomial (x4 + x + 1) 0x2 = Pseudo-Random Polynomial (x4 + x3 + 1) 0x3 = Pseudo-Random Polynomial (Alternating "x4 + x + 1" and "x4 + x3 + 1" every cycle)

BITFIELD	BITS	DESCRIPTION	DECODE
M2_FSREN	1	Buck Master2 Falling Slew-Rate Control	0x0 = Disable (Buck does not sink current from C_{OUT} in SKIP or LP-SKIP mode) 0x1 = Enable (Buck operates in FPWM mode to sink current from C_{OUT} when its $V_{OUT(TARGET)}$ is lower than the actual V_{OUT})
M2_FPWM	0	Buck Master2 Forced-PWM Control	0x0 = Disable (Automatic SKIP mode operation under light load condition) 0x1 = Enable ('OR' Logic with FPWM2B input)

M2_CFG3 (0x37)

BIT	7	6	5	4	3	2	1	0
Field	M2_ADIS100	M2_ADIS1	M2_ULTRA	M2_FTRAK	M2_FREQ[1:0]		M2_ILIM[1:0]	
Reset	0x1	0x0	0x0	0x0	0x1		0x3	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
M2_ADIS100	7	Buck Master2 100Ω Active Discharge	0x0 = Disable 0x1 = Enable
M2_ADIS1	6	Buck Master2 1Ω Active Discharge. Note that 1Ω active discharge must be disabled when falling slew-rate function of corresponding output is disabled (M2_FSREN = 0).	0x0 = Disable 0x1 = Enable (Active for 1ms after Soft-stop is completed)
M2_ULTRA	5	Buck Master2 Ultrasonic Mode Control	0x0 = Disable 0x1 = Enable
M2_FTRAK	4	Buck Master2 Internal Frequency Tracking Control	0x0 = Disable 0x1 = Enable
M2_FREQ	3:2	Buck Master2 Switching Frequency Setting	0x0 = 0.5MHz 0x1 = 1.0MHz 0x2 = 1.6MHz 0x3 = 1.6MHz
M2_ILIM	1:0	Buck Master2 Peak Current Limit Setting	0x0 = 1.50A 0x1 = 2.25A 0x2 = 3.00A 0x3 = 4.50A

Applications Information—Dual-Phase Configurable Buck Converter

Inductor Selection

An inductor with a saturation current that is greater than or equal to the peak current limit setting (I_{PLIM}) is recommended. The load current requirement (per phase) of the system is also considered to choose the RMS current rating of the inductor. Inductors with lower saturation current and higher DCR ratings tend to be physically small, however higher values of DCR reduce the efficiency. To choose a suitable inductor for the given application, trade-off the size of the inductor and the DCR value. It is recommended to choose an inductance such that the inductor's ripple current to the average current ratio is between 30% and 60%. Consider the output voltage range when choosing the inductance; in general, 0.47μH are suitable for low-range outputs, 1.0μH are suitable for mid-range outputs, and 1.5μH are suitable for high-range outputs. Note that higher inductances slow down the maximum slew rate of the inductor current, and high duty cycles (V_{IN} close to V_{OUT}) coupled with large inductance can slow down the load transient response.

Table 11. Recommended Inductors

MANUFACTURER P/N	INDUCTANCE (μH)	TYPYCAL DCR (mΩ)	TYPYCAL I_{SAT} (A)	TYPICAL I_{TEMP} (A)	DIMENSION (L x W x H) (mm)
DFE252012F-R47M	0.47 ±20%	23	6.7	4.9	2.5 x 2.0 x 1.2
DFE252012F-1R0M	1.0 ±20%	40	4.7	3.3	2.5 x 2.0 x 1.2
DFE252012F-1R5M	1.5 ±20%	58	3.8	2.7	2.5 x 2.0 x 1.2

For the dual-phase configuration, each phase needs its own inductor with the same inductance value (do not short the LX nodes of different phases together on the PCB). See the *Phase Configuration* section for more information regarding different phase configurations.

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the battery or input power source and reduces switching noise in the device. The impedance of the C_{IN} at the switching frequency should be kept very low. Ceramic capacitors with X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications, a 10μF capacitor is sufficient.

Output Capacitor Selection

The output capacitor (C_{OUT}) is required to keep the output voltage ripple small and to ensure the regulation loop stability. The C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors with X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. The recommended minimum effective output capacitance **per phase** is shown as follows:

Table 12. Recommended Minimum Effective Output Capacitance

V_{OUT} RANGE	SWITCHING FREQUENCY (MHz)	MINIMUM EFFECTIVE C_{OUT}* (μF)
Low (0.3V - 1.2V)	1	42
Mid (1.0V - 2.4V)	1	24
High (2.0V - 5.2V)	1	16
* The required minimum $C_{OUT(EFF)}$ is inversely proportional to the switching frequency. For example, an output using RNG = 0 and 1MHz switching frequency requires a minimum of 42μF of effective output capacitance. Changing the switching frequency to 1.6MHz increases the C_{OUT} requirement to 27μF (42μF/1.6).		

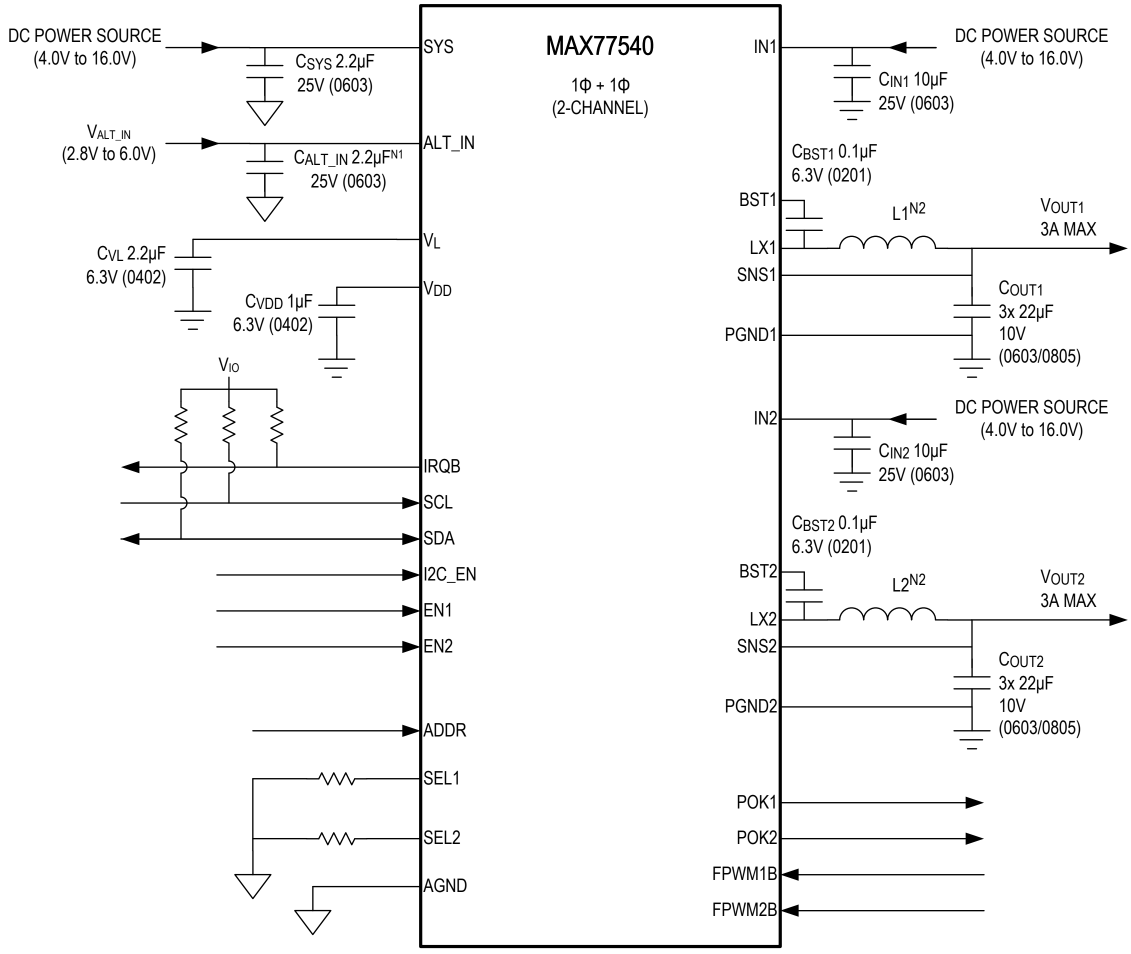
The effective C_{OUT} is the actual capacitance value seen by the Buck output during operation. The nominal capacitance (C_{OUT}) needs to be selected carefully by considering the capacitor's initial tolerance, variation with temperature, and derating with DC bias. Refer to *Tutorial 5527* for more information. Larger values of the C_{OUT} (above the required minimum effective) improve load transient performance, but increase the input inrush currents during startup. The output filter capacitor must have low enough ESR to meet output ripple and load transient requirements. The output capacitance must be high enough to absorb the inductor energy while transitioning from full-load to no-load conditions. When using high-capacitance, low-ESR capacitors, the filter capacitor's ESR dominates the output voltage ripple in CCM. Therefore, the size of the output capacitor depends on the maximum ESR required to meet the output voltage ripple specifications.

General PCB Layout Guidelines

- The power components should be placed first and then small analog control signals.
- It is important to always have a ground layer next to the power stage layer because a solid ground layer provides uninterrupted ground return path between the input and the output caps during switch on-time. (A solid plane minimizes inductance to the absolute minimum and also is a very good thermal conductor and can act as a heat sink.)
- It is recommended to have thick copper for the external high current power layers to minimize the PCB conduction loss and thermal impedance.
- The power stage loop that is made by the input capacitor (C_{IN}), the LX trace, the inductor (L), and the output capacitor (C_{OUT}) coming back to the PGNDx bumps should be minimized for electromagnetic compatibility (EMC) considerations.
- The input capacitors (C_{IN}) should be located close to the input bumps of each phase.
- Bypass capacitors for the V_L, the V_{DD}, and the BSTx pins should be placed as close as possible.
- Analog ground (AGND) and power ground (PGND) bumps should be directly connected to the ground plane separately in order to avoid common impedance ground.
- It is recommended to avoid having direct connection the SYS and its AGND traces to the nearest IN and the PGND traces.
- The output voltage sensing trace should not intersect the power stage (the loop made by the input capacitor, LX trace, inductor, output capacitor, and the PGND)
- It is important to have impedance matching between phases for stable operation in multiphase configuration. (The output PCB trace of each phase should be as symmetric as possible.)
- For multiphase configurations, the output voltage sensing bumps for the master phase should be connected to the middle point of the output phases.

Typical Application Circuits

1+1 Phase Configuration with I^{2}C Enabled



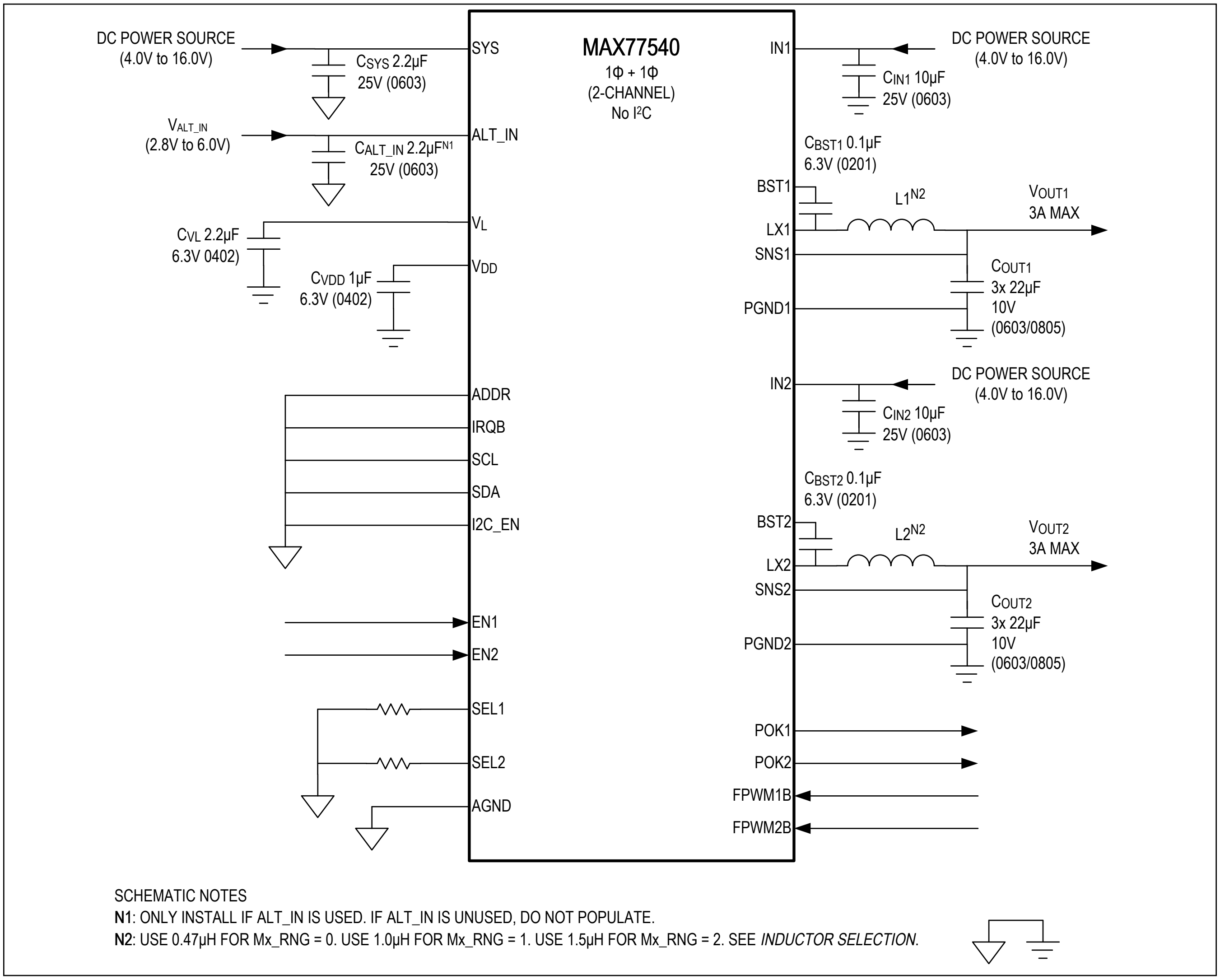
SCHEMATIC NOTES

N1: ONLY INSTALL IF ALT_IN IS USED. IF ALT_IN IS UNUSED, DO NOT POPULATE.

N2: USE 0.47µH FOR Mx_RNG = 0. USE 1.0µH FOR Mx_RNG = 1. USE 1.5µH FOR Mx_RNG = 2. SEE *INDUCTOR SELECTION*.

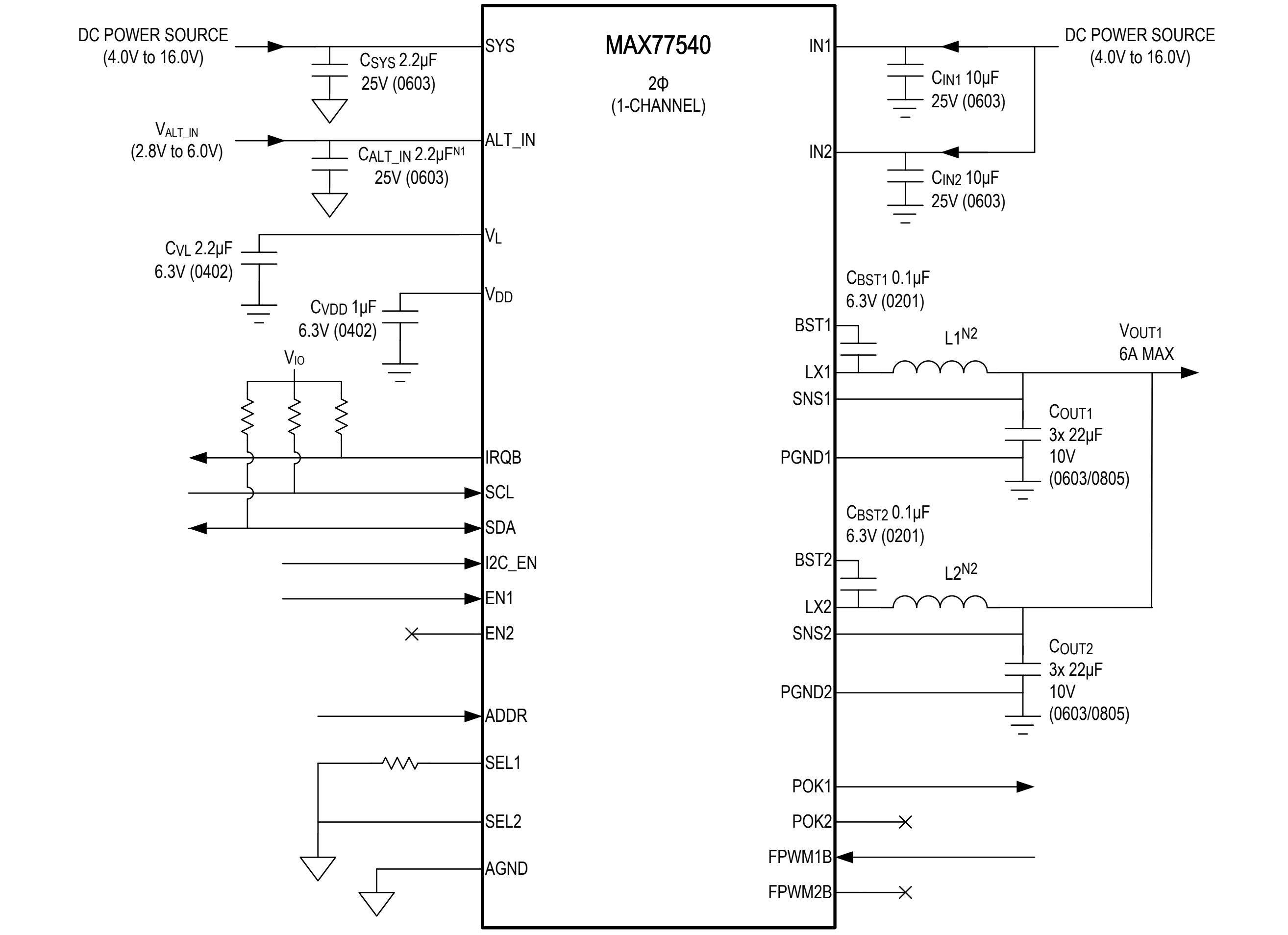
Typical Application Circuits (continued)

1+1 Phase Configuration without I²C



Typical Application Circuits (continued)

Dual-Phase Configuration with I²C Enabled



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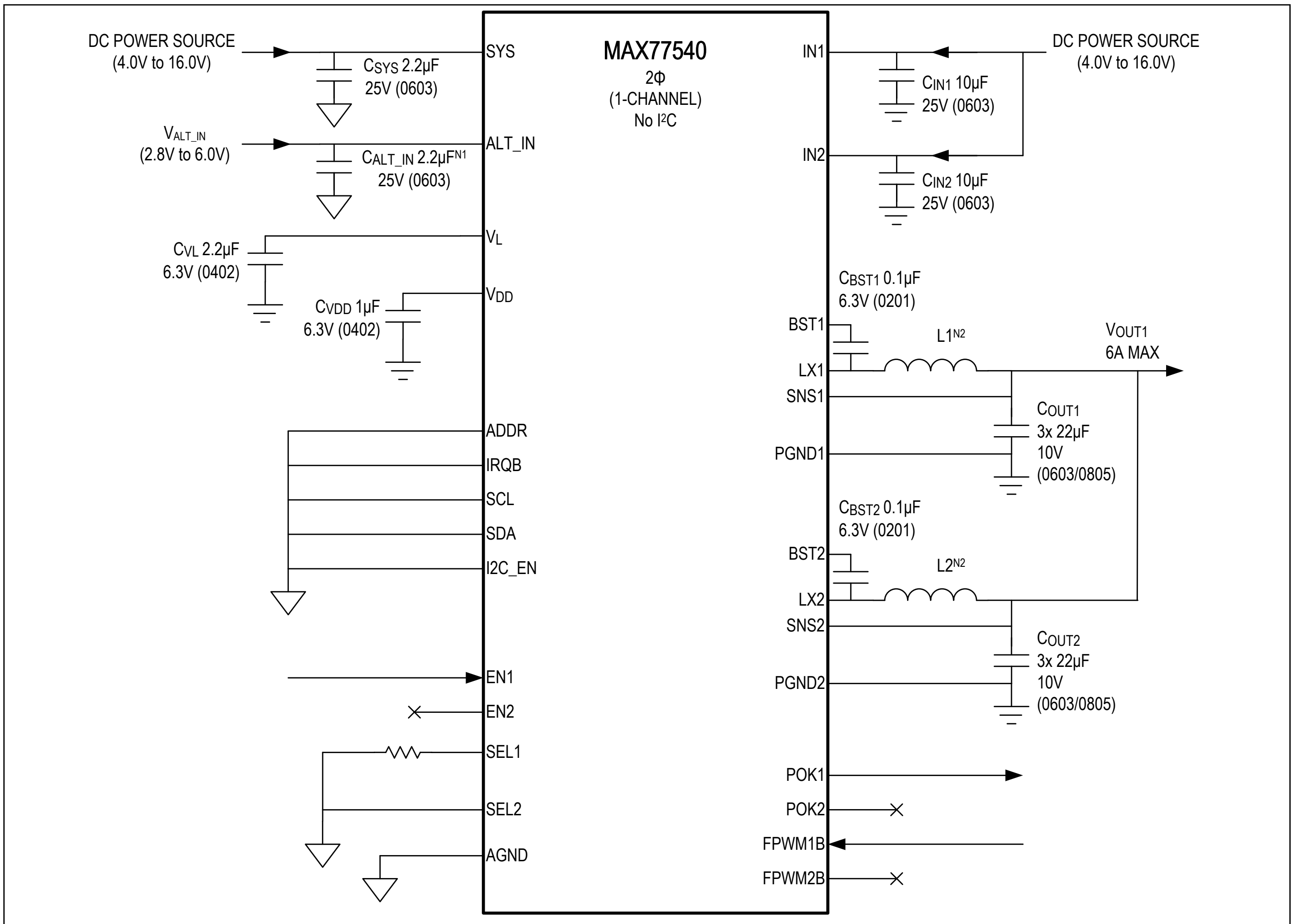
N3: EN2, POK2, FPWM2 ARE ALL SHOWN AS 'NO CONNECT' BECAUSE THEY ARE UNUSED IN 2-PHASE CONFIGURATION.

Typical Application Circuits (continued)

Dual-Phase Configuration without I^{2}C



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N1: ONLY INSTALL IF ALT_IN IS USED. IF ALT_IN IS UNUSED, DO NOT POPULATE.
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N3: EN2, POK2, FPWM2 ARE ALL SHOWN AS ‘NO CONNECT’ BECAUSE THEY ARE UNUSED IN 2-PHASE CONFIGURATION.

Ordering Information

PART NUMBER	FACTORY OPTION	PIN-PACKAGE
MAX77540AAWV+T	A	30 WLP
MAX77540AAFG+T*	A	24 FC2QFN

T = Tape and reel.

** Future product. Contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/21	Release for market intro	—